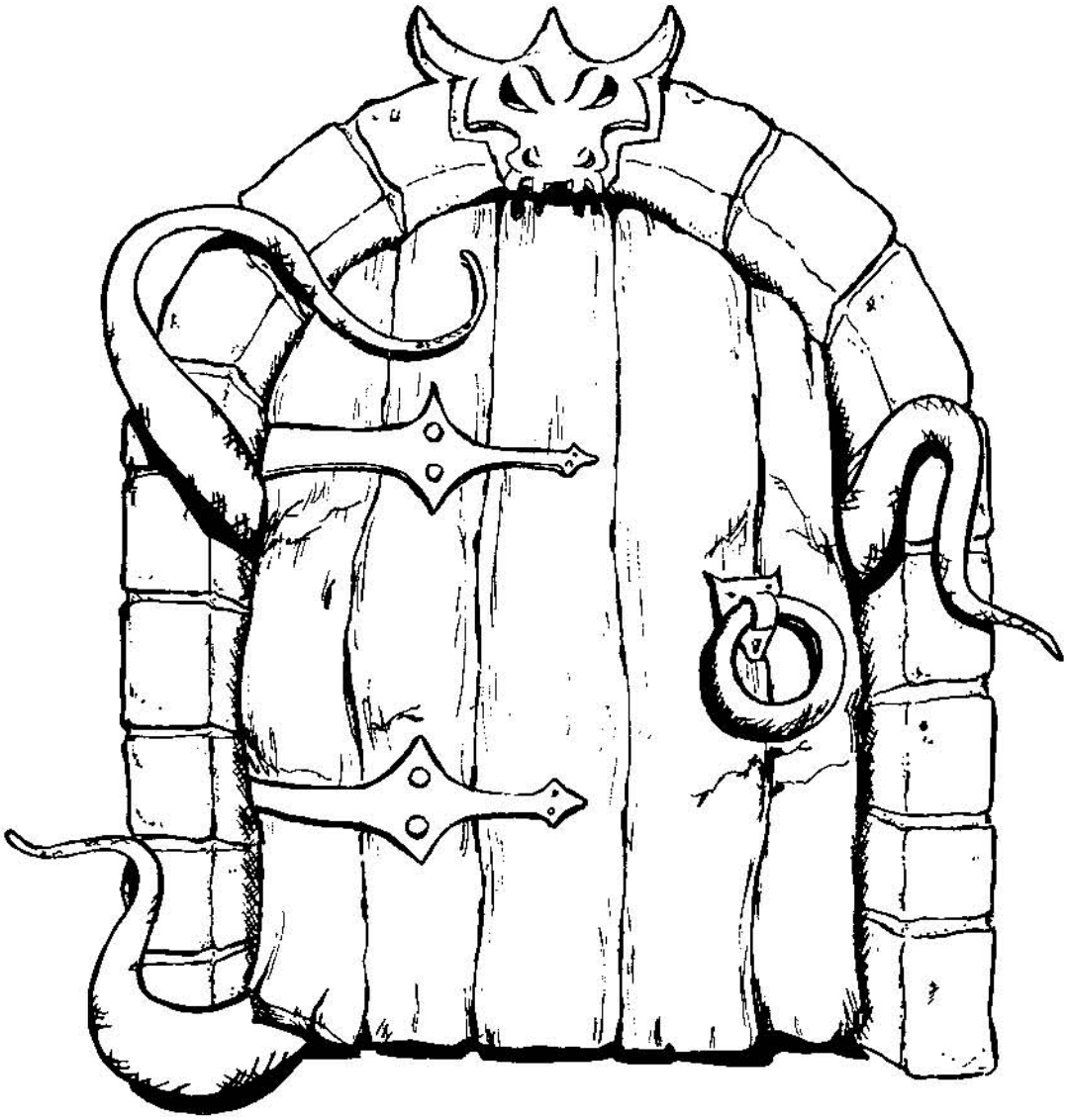
Venture™

Technical Manual 2.0



Exidy

VENTURE (TM)

Technical Manual 2.0

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EXIDY VENTURE (TM)

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FOREWORD

In keeping with the progress Exidy has made to satisfy the needs of all those involved with the operation of an Exidy video game, we have duplicated especially pertinent information in both our Operator and Technical manuals. For example, we now are including a complete Parts List and accompanying drawings in both manuals. That way should you need to separate the manuals, the VENTURE™ Technical Manual, Version 2.0, contains all the information a technician needs to service VENTURE™. The Operator's manual, then, contains all information necessary for installation and routine running of VENTURE™.

We have designed the Technical manual to aid in your understanding of schematics. Each board schematic (logic, audio/color, and memory expansion) is accompanied by a description directly opposite it. These are sectioned by the page number of the drawing they describe.

After the board schematic drawings and descriptions, we provide information on Audio Diagnostic Test, Power Supply, Joystick and Audio adjustments. An illustrated parts list follows.

Exidy welcomes your suggestions for more ways to make provide you convenience. Please use our toll free number (800) 538-8402. We'd welcome your ideas.

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1. Master Oscillator (1D)

From this oscillator all dynamic operations are derived, such as the processor clock, the main element and line counters, the shift register clocks, as well as all other forms of timing signals.

2. Element (Horizontal) Counters (1C, 1E, 2E)

These components form the final stages of horizontal timing. All operations in this game requiring horizontal positioning or timing have their origin here. Note that, beginning with signal HCLK (from Clock Divide Counter 2D), there are 256 counts prior to setting signal E256 high. When this signal goes high, it indicates that the horizontal blanking period is in progress. At this time the final counter (1E) is preloaded with a higher number than previously loaded. This creates a shorter count the second time around. The shorter count measures the retrace interval. When the retrace count is finished, the counter preloads with a lower number, establishing a longer count sequence again for "real time" sweep of the electron beam across the face of the CRT.

3. Line (Vertical) Counters (4F, 5F, 6E)

These components form the entire vertical timing operation starting with a clock derived from horizontal timing. These counters count 256 times and then preload with a higher number, causing a shorter count the second time. This shorter count measures the vertical retrace interval. Note that signal L256, when high, indicates vertical blanking is in progress. After the completion of the vertical retrace count, the counters once again preload with a lower number. This way they count 256 times during the sweep of the electron beam down the face of the CRT, allowing the horizontal timers to sweep one complete horizontal line for each count of the vertical counters. Thus, the electron beam reaches the bottom of the CRT, after completing 256 horizontal line sweeps. It then begins the vertical retrace count, and the whole cycle begins anew with the beam starting again at the top of the CRT.

4. Screen RAM Addresses (7D)

During the time the screen RAM is examined by the logic for output to the monitor screen, addresses must be applied to the screen RAM to count up at a rate corresponding to the image cells conceptually arranged on the screen in a 32 x 32 matrix. The counts used here, 4 from the element counters, and 4 from the line counters, fulfill this timing requirement. The least significant element count used (E8) represents an interval exactly eight times that of one element. The least significant line count used represents an interval exactly eight times that of one horizontal line, or eight times a single line count. Dividing a 256 element line by 8 yields 32, and likewise dividing a 256 line vertical sweep by 8 yields 32. Thus the screen RAM address lines (RAM0 through RAM9) count at a rate that creates 32 horizontal counts and 32 vertical counts as the electron beam sweeps the face of the CRT. This makes 1024 conceptual "image cells" into which can then be inserted images of 8 elements by 8 lines. For more information concerning these images, refer to the text for pages 2 and 3 of the Logic Schematics.

5. Coin Input Decoding (1H)

Some models of VENTURE (TM) contain two separate coin inputs for special coinage applications. NOR gate 1H combines these separate inputs, making signal 5COINT, which sets the interrupt flip-flop (6E on page 8) when either coin input becomes active, thus forcing the microprocessor to jump to the interrupt service routine. This interrupt driven operation prevents ever missing a coin when inserted. However, this also means that when a game is first powered up, the coin input must be inactive. If for some reason the coin input switch is enabled at the time of power up, the game does not properly initialize until the switch is disabled.

6. Hardware Generated Line Positioning Proms (3E, 4E)

These PROMs are not used for VENTURE (TM).

7. Blanking and Video Clocking (5H)

Flip-flop 5H merely combines blanking and all other video.

8. Black and White Composite Video Output (1H)

This circuit is not used for VENTURE (TM). If desired, however, these components may be installed to aid troubleshooting, by acting as a "video probe".

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1. Screen Controller PROM (6D)

This PROM controls the direction of data flow into and out of the screen RAM and character generator RAM. It prevents timing errors and buss conflicts, assuring that the microprocessor can write to either the screen or character generator RAM, or read back from either.

2. Screen RAM (7B, 8B)

The screen RAM is comprised of two 1024 x 4 static RAMs, configured to act as a single 1024 x 8 RAM. This creates a screen matrix of 32 horizontal by 32 vertical positions. A single byte code is stored in each of these positions to represent a particular character. During "real time" (the time the CRT is being swept by the electron beam) these character codes address the character generator RAM.

These character codes, when used as addresses, are combined with the three least significant line counts (L1, L2, L4) to present to the character generator output shift register all the necessary data to form an 8 element wide by 8 line high character on the CRT, located within one of the 1024 positions mentioned immediately above; that is, the 32 horizontal by 32 vertical positions.

The screen, then, is a storage place for single byte codes that call up an 8 x 8 character and place it into the corresponding character cell. This character is stored in the character generator RAM, shown on page 3 of the schematic.

3. Character Image Storage

Shown on this page are two PROMs (9C, 10C). They could be used as a permanent set of characters. However, VENTURE (TM) uses RAM instead, to increase the flexibility in character manipulation. This portion of RAM appears on page 3 of the Logic schematics.

4. PROM Power and Signal Selection (10B)

This Dip Shunt configures the logic for different types of PROM devices. For VENTURE (TM), however, this Dip Shunt is unnecessary due to the fact that RAM has been used rather than PROM.

5. Character Generator Output Shift Register (12B)

Video from the character generator memory devices (RAM in the case of VENTURE (TM)) is formed by this shift register as a byte of data that displays one line at a time from left to right on the CRT. This ultimately forms an 8 line high by 8 element wide character positioned on the screen according to the time it is presented to the shift register.

Output from this shift register are all the images seen on the screen except the player image and the player missile image.

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Image Storage RAM

1. Character Generator Image Storage RAM (13C, 11C, 14C, 12C)

These four RAMs, when used in this configuration, act as a 2048 x 8 bit RAM. The images placed on the screen are stored in this RAM by the microprocessor, according to the game program. In this RAM images are established, altered, shifted slightly, and even replaced with a new set, if required by the program.

When called by the logic to do so, the RAM presents, to the character generator shift register, a single byte, representing one line of a particular image. Each image is composed of 8 lines of data, each line is one byte-wide. Thus, 256 images of 8 x 8 bits can be stored here simultaneously and "called up" by the screen RAM to be displayed on the CRT in any of the 1024 character cell positions. A single byte code, stored in the screen RAM, calls up a character. The character may change or move by replacing the single byte code in the screen RAM, or by altering the data in the character generator RAM which forms the image.

PAGE 4 OF 8, GAME LOGIC PCB

1. The 6502 Microprocessor (2A)

For detailed information concerning this microprocessor, refer to the MOSTEK publication, 6500-10A, MCS Microcomputer Family Hardware Manual.

One feature that should be mentioned here, however, is that this microprocessor has 'memory-mapped I/O'. This means that all ports interfacing to peripherals of any type must be located within the normal memory map, with no duplication of addresses, since no instructions are specifically oriented toward I/O operations.

2. Power-on Reset circuit (connected to 2A pin 40)

When power is first applied to a game, a particular sequence of events must occur to set up all logic conditions. If this sequence is broken for whatever reason, the microprocessor may become confused, and the game will not start and run.

This sequence is accomplished when the reset line to the microprocessor is the last line allowed to reach a 'high' logic level. The Power-on reset circuit makes sure this occurs by utilizing the charge time of an RC network as a delay.

If any kind of power interruption occurs during normal game play, the power-on reset circuit insures that the microprocessor is reset. This alleviates confusing the microprocessor, while it also recreates the original power-on sequence.

3. Processor Workspace RAM (4A, 5A)

The RAM, or workspace, consists of the lowest 1024 bytes of memory and can be divided into three separate sections due to distinctly different functions.

The lowest 256 bytes (0 to FF Hexadecimal) is reserved for special software register operations, and is called 'zero page'. The processor uses this area to store dynamic variables. For details of this type of operation, refer to 6502 technical literature regarding 'Zero Page Addressing'.

The next higher 256 bytes (100 to 1FF Hex) is reserved for the 6502 stack. The processor stores return addresses in the stack when interrupted or called to execute a subroutine. The game program may also request the processor to store other kinds of information here for later retrieval.

The next higher 512 bytes (200 to 3FF Hex) are used as a scratchpad area. Miscellaneous calculations and their results are temporarily stored here.

4. Main Address Decoding (5C, 5D, 5E)

This circuit is the first stage of the address line decoding necessary to organize the memory map; that is, it places specific functions or devices within generalized blocks of the memory map, grouped by function.

For details on the addressing scheme, see MEMORY MAP, Figure 1.

PAGE 5 OF 8, GAME LOGIC PCB

1. Program Memory (6A through 13A)

These memory devices may be 2516, 2716 (5 volt only), or 2732 EPROMS. If 2516 or 2716 EPROMS are used, there will also be an additional memory expansion PCB in use to create more memory space. This PCB is simply an extension of the address, data and control lines present at the memory devices situated on the logic PCB.

Note that four of the lines to each memory device (PCS0 through PCS7, PAP19, PAP20, PAP21) are programmable through jumper configurations located at 4B and 11B. This allows different memory devices to be used and/or facilitates interconnection to the memory expansion PCB (if used).

2. PROM Address Selection (4B, 5B)

This is a second stage of address decoding, used to select each individual memory device when addressed. Signal ROMSEL (from page 4 Main Address Decoding) selects the Program Memory devices in general, and jumper 4B, together with decoder 5B further defines an address to a particular memory device.

3. Memory Device "Personality" Selection (11B)

The dip shunt, or jumpers block, alters control signal configuration to the program memory devices. This allows the use of alternate size EPROMS and/or those created by different manufacturers whose control signal pinouts may not be identical to one another.

1. Moving Object Horizontal Position (13F, 15F, 14F, 16F)

Counters 13F and 15F form a byte-wide counter which horizontally positions Moving Object 1 on the screen. These counters are preloaded to a certain value by the microprocessor during Vertical Retrace time. Then, after each occurrence of the Horizontal Sync, they begin to count. The count outputs AND'ed through 15E give rise to signal M1HW, the Horizontal Position Window for Moving Object 1. Counters 14F and 16F are the equivalent circuit for Moving Object 2.

2. Moving Object Vertical Position Counters (16E, 12E, 1E, 13E)

Counters 16E and 12E form a byte-wide counter which positions Moving Object 1 vertically on the screen. These counters are preloaded to a certain value by the microprocessor during Vertical Retrace time. Then, after each occurrence of Vertical sync, they begin counting. The four count outputs of the least significant of these two counters (M1L1, M1L2, M1L3, M1L4) are sent to the moving object image PROM to specify which line of the image is presently being displayed. The AND'ed outputs of the second counter give rise to signal M1VW, the Vertical Position Window for Moving Object 1. Counters 11E and 13E are the equivalent circuit for Moving Object 2.

3. "Write Moving Object" Decoding (6F, 16H, 5E, 3F)

Consists of two distinctly different functions. 6F and 16H form the circuit that generates the load pulses for the moving object position counters, while 5E and 3F simply prevent the counters from counting during blanking.

4. Color Interface Output (16B)

This is a 14 pin DIP socket used as the connector interface to the color selection circuitry, located on the audio PCB. The signals and their functions are listed below:

Pin #		
1	5SRLOAD	= Shift Register Load Pulse (Neg. True)
2	CBLB	= Composite Blanking
3	CSYNC	= Composite Sync
4	5CVID	= Composite Video (Neg. True)
5	5SCLK	= Shift Register CLock (Neg. True)
6	HSYNC	= Horizontal Sync
7	GND	
8	VSYNC	= Vertical Sync
9	5MO2VID	= Moving Object 2 Video (Neg. True)
10	5MO1VID	= Moving Object 1 Video (Neg. True)
11	VA9	= Character Generator Address Line 9
12	5LINES	= NOT USED ON VENTURE
13	VD7A10	= Character Generator Address Line 10
	+5V	

1. Moving Object Multiplexing (14A, 14E)

These two multiplexers pass information to the moving objects image PROM. They contain two codes: one determines which image should appear, and the other specifies which line of that image is to be displayed.

The data passed alternates between data for Moving Object 1 and Moving Object 2, depending on the state of element count E32.

The upper multiplexer (14A) passes the "which image" code, and the lower multiplexer (14E) passes the "which line of that image" code.

2. Moving Objects Image PROM (11D)

This EPROM accepts as an address the image and line codes of moving objects 1 and 2 (see "Moving Object Multiplexing" above). It then presents the appropriate data for one line of the image to the output shift registers.

The timing of the logic insures that the correct pair of shift registers are loaded with the data, then shifted out at the correct time to become, one line at a time, the 16 lines of video for that character (Moving Object 1 or 2).

3. Moving Object Video Output Shift Registers (12D, 13D, 14D, 15D)

Shift registers 12D and 13D together form a 16 bit shift register whose task is to accept, as data, 16 bits (2 bytes) representing a single line of the image for Moving Object 1, then shift these 16 parallel bits out serially to become video. This operation is repeated for 16 consecutive lines, resulting in a video image that is 16 bits wide by 16 lines high on the monitor screen.

Shift registers 14D and 15D together form this same type of circuit, identical in function, for Moving Object 2.

4. Moving Objects Shift Register Load Logic (2F, 16H)

This circuit sends properly timed load signals to the Moving Object Video Shift Registers. These load signals are needed to load the image data into the shift registers at locations 12D, 13D, 14D, and 15D.

5. Moving Object Shift Register Control Logic (15H, 14H)

The input signals to the upper two gates (15H) represent horizontal and vertical position "windows" for the two moving objects (for example, M1HW = Moving Object 1 Horizontal Window, M2VW = Moving Object 2 Vertical Window). These windows allow the Moving Object shift registers to shift only at the right time. This insures the image is generated at the correct position on the screen.

The lower 2 gates of 15H are, in VENTURE, used for later decoding in the color selection circuitry, located on the audio PCB.

6. Memory Device Personality Configuration (10D)

This is another Dip Shunt which reconfigures the PC board in order to use an EPROM (11D) of another type or manufacturer.

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1. Interrupt Status Latch (8E)

This latch is set when a coin is dropped or vertical sync occurs. When the latch is set, the CPU is interrupted; that is, signal $\overline{IRQ}$ goes low. This forces the CPU to jump to the interrupt service routine. The interrupt service routine instructs the CPU to check for a coin input, and then run a debounce routine on the coin bits of ports 9E or 15A, depending on which coin input bit was set at 8E.

If the CPU finds no coin input bit set at latch 8E, it will assume the Interrupt condition was caused by vertical sync. This tells the CPU that it should now jump to the routine that services the normal game play, and that the screen can now be updated with new data. The screen can only be updated during the vertical retrace interval.

Note that this latch also has two signals labeled LNG0 and LNG1 which both show PC etched jumpers. These two bits are the select bits for one of four languages, English, French, German, and Spanish. You may select a language by cutting the appropriate jumper, allowing it to be pulled to a logic high. For English, no cutting is necessary. See the Operator's Manual for proper configuration of other languages.

Also on this latch is the signal named TABLE. This signal, tied to a pullup resistor and switch, determines whether the program operates as a table model or in the upright game configuration. Please check with the Exidy Marketing Department and the Operator's Manual for more details, since table models may or may not be available.

2. Option Switch Port (15A)

This port provides input from the option dipswitch, at location 16A. Data from the dipswitch is gated onto the data buss and read by the CPU at game start. This allows such options as number of turns, coins per game, additional game versus extra turn, etc.

Note that one input of this port (labeled COIN 2) does not come from the switch. Instead, it comes from Coin Input 2, and is used for debouncing the auxiliary coin input switch.

3. Control Inputs Port (9E)

This port provides input from the controls located on the control panel, such as the joystick, fire button, one player start, and two player start. Data from these controls are gated onto the data buss for examination by the CPU during the regular service routine (which is synchronized to the vertical interval).

Note that one of these inputs is from the COIN1 input (labeled 5COIN1) rather than a game control input. The COIN1 input to this port is used for debouncing the standard coin input.

4. Moving Image Latch

Only the CPU can write to the moving image latch. This latch contains the code that specifies which image or images are presently being displayed by the hardware moving object circuitry.

5. Audio Board Port

This latch is written to and read by the CPU, and transmits instructions to the audio board when any sounds are enabled, disabled, or the game is initialized. In addition, this port passes data sent to select colors for screen images. For the functions of these instructions, see the audio board schematic and/or description of operation.

6. Control Port Latch (9D)

This latch, used only in table versions, is written to only by the CPU and keeps track of which player is "up", in order to select which controls are active, that is, player one or player two.

7. I/O Decoding (7E)

The upper half of this decoder generates the chip selects for those I/O devices written to by the CPU, and the lower half generates the chip selects for those I/O devices which are read by the CPU. See the detailed memory map for more precise information.

Figure 1: MEMORY MAP

Hex Address	Function or Device
FFFA-FFFF	Interrupt and Reset Vectors
8000-FFF9	Program memory space
52XX	Audio board communications
5103	Interrupt Condition Latch (read)
5101	Control Inputs Port (read)
5101	Output Control Latch (write) (Not used in VENTURE (TM) upright)
5100	Moving Objects Image Latch (write)
5100	Option Dipswitch Port (read)
50C0	Moving Object 2 Vertical Position Latch (write)
5080	Moving Object 2 Horizontal Position Latch (write)
5040	Moving Object 1 Vertical Position Latch (write)
5000	Moving Object 1 Horizontal Position Latch (write)
4800-4FFF	Character Generator RAM
4000-43FF	Screen RAM
0200-03FF	Scratchpad RAM
0100-01FF	Stack RAM
0000-00FF	Zero Page RAM

AUDIO/COLOR PCB-GENERAL DESCRIPTION

The Audio/Color PCB is so named because it contains not only the circuitry required to generate all sounds, but also the color selection decoding circuitry and video output connector.

This PCB contains a dedicated 6502 microprocessor and circuitry to support the simultaneous generation of many types of sound, including three channel music. The Logic PCB simply sends commands to the Audio/Color PCB via a bi-directional communications port and the Audio/Color PCB takes it from there. In some cases this PCB even aids the Logic PCB in some of it's calculations when there is not enough processing time available on the Logic PCB.

As a result of this structure, the actual program to generate sounds or music resides on the Audio/Color PCB. There is also a handshake required between the two PCB's in order for the system to power up correctly, and of course, there is no video output without the Audio/Color PCB connected.

PAGE 1 OF 5, AUDIO/COLOR PCB

1. Logic and Power Interface (P5, J2, J3)

Connector P5 provides the audio/color PCB with all the power it requires to operate. Also fed through this connector are the two speaker output leads. P5 interfaces only to the power supply module and the speaker, through the main harness.

Connectors J2 and J3 are the most significant path of communication between the Logic and Audio/Color PCB's. Address lines, Bi-directional Data lines, processor control lines, and the Audio/Color PCB Select line are all passed through these two connectors.

2. Communications and Address Decoding (9B, 13D)

Peripheral Interface Adapter (PIA) 9B, in concert with 8B (another PIA, shown on page two) serves as a bi-directional communications path between the Logic PCB and the Audio/Color PCB. During information transfer between the two PCB's, both PIA's are in use. Information from the Logic PCB microprocessor passes through the PIA at 9B to the PIA at 8B, then to the microprocessor on the Audio/Color PCB. When information is passed the other direction, the path is the same, but the direction is reversed.

During the time that no information transfer is occurring between the two PCB's, both microprocessors can continue to operate independently.

Also shown on page one is 13D, a 3-line to 8-line decoder, used to generate the write signals for the Color Data Latches. These Latches will be covered in the text for page five of the Audio/Color PCB.

1. 6502 Microprocessor (3B)

This microprocessor is the same as that used on the Logic PCB, but is exclusively dedicated to the generation of sound. It can communicate with the Logic PCB microprocessor, and receives it's instructions thereby. Once it has received it's instructions, however, it asserts complete control over all Audio/Color PCB circuitry and ignores the Logic PCB microprocessor until such time as it is informed that another command is ready. Some commands are of a type that must be processed immediately, irregardless of other operations in progress, and some commands can wait until the operations in progress are completed. The program on the Audio/-Color PCB handles all these eventualities appropriately.

2. Peripheral Interface Adapters (8B, 7B)

The PIA at 8B, as mentioned in the text for page one, is used in bi-directional communications between the microprocessors on the Logic PCB and the Audio/Color PCB.

The PIA at 7B is used for two fundamental purposes on this PCB. The first, and most important, is that it contains the RAM that the microprocessor uses for zero page and stack operations. The PIA only contains 128 bytes of RAM, which under normal circumstances would not be sufficient for both zero page and stack. In this case, however, the memory map on this PCB has been altered, so that when the microprocessor thinks it is putting the stack at address 01FFH it is actually putting it at address 007FH.

The second use of this device is that of a programmable interval timer, used for various purposes unique to the specific sounds being generated on this game. The ability of this device to generate interrupts at time out is utilized here.

3. Address Decoding (4B)

Keyboard Encoder (4B) is used here to generate the chip selects of all devices located in the memory map of the Audio/Color PCB.

4. Music Generator (2B)

Another Programmable Counter/Timer device is used here to generate music (and sometimes other special effects) in up to three channels (or voices) simultaneously. The music is created by a special software operating system, and all but the counter/timer chip is therefore invisible.

5. Master Oscillator (A1,B1)

This oscillator is the source of all timing on the Audio/Color PCB. If this clock stops running, so does everything else on the Audio/Color PCB. It is, however, completely independent of the clock and other timing signals generated by the Master Oscillator located on the Logic PCB.

6. Program Memory (3A, 4A, 5A, 6A, 7A)

The memory devices used here are 2716 (2048 x 8) EPROMS. The DIP shunt located at 8A is used to reconfigure the control and power supply lines, if necessary, for equivalent devices from different manufacturers, whose pinouts may not be the same.

7. Output Filter Latch (1C)

This latch is used simply to switch different output filter capacitors in or out of the circuit to soften or shade the sound, according to program requirements.

PAGE 3 OF 5: AUDIO/COLOR PCB

1. Clock Manipulation and Noise Generation Circuit (3D,4D,6D,5E)

The timers inside Programmable Timer Module 3D can be incremented or decremented either internally by the Phase Two clock input, or externally from the 'C' inputs (C1,C2,C3). Both options are used by the program. When the counters are being controlled by the Phase Two clock, the 'C' inputs have no effect, and the noise generation circuit is therefore inoperative. In order to generate sounds that are classified as noise, or contain some kind of noise within them, the counters are programmed to decrement in accordance with the input on the 'C' inputs. While in this mode, the combination of 6D (Dual 'D' Flip-Flop) and 5E (128 Bit Shift Register), are used to 'randomize' the clock inputs to the Programmable Timer Module (3D). The 'randomizer' can be clocked with either the Phase Two clock or counter output Q1.

2. Amplitude Modulation Control (2D, 7D, 8D, 9D)

Counter (3D) outputs Q1,Q2, and Q3 are already highly complex sounds, but in order to create much more specialized audio they must be modulated in amplitude. Each channel is separately controllable in amplitude by associated Digital-to-Analog converters comprised of analog multiplexers and a resistive ladder network. Three control bits on each multiplexer select a voltage to output, according to which input pin is addressed (since each input pin is tied to a different point, and therefore voltage, in the resistive ladder).

The voltage thus selected is applied to one of the two inputs to each segment of 2D (another triple analog switch). The other input is tied to ground. Note that the control bit to each analog switch segment is one of the previously mentioned count outputs (Q1,Q2,Q3). In this manner, each output can be controlled for frequency and amplitude individually.

Note also that the count output from Q1, unlike Q2 and Q3, first passes through yet another analog switch whose function is to turn off the count output of Q1 prior to reaching the Digital-to-Analog conversion stage. This is done because the Q1 output is the one used for selective clock frequency generation, and would therefore interfere with other sounds if not disabled at the appropriate time.

3. Output Summation and Special Effects Volume Control (2E)

The three segments of Operational Amplifier 2E are configured as voltage followers (for impedance considerations), and their outputs are summed together at the top of a 10K POT, R31. The output volume, therefore is determined by the voltage applied at each input and the adjustment of the POT. Note that the resistors used to sum these three outputs together are large in value, so that each channel will have minimal effect on the others when conflicting signals arrive simultaneously (except, of course, that their sum will appear at the output).

This summed output is then again summed with all other sounds generated by this PCB at the input to the final Power Amplifier.

PAGE 4 OF 5: AUDIO/COLOR PCB

1. Summing Amplifier and Master Volume Control (3F, R46)

One segment of Operational Amplifier 3F is used here as a point at which all the various sounds generated on this PCB are brought together. Note that the output goes immediately to a 10K POT (R46) which has ground on the other end. The wiper, therefore, varies the final output volume of all sounds together.

2. Integrator and Audio Power Amplifier (3F,10F)

Another segment of Operational Amplifier 3F is used here as an integrator; that is, it is used to 'roll off' the higher frequency sounds in order to prevent the power amplifier from going into unwanted oscillation.

The Audio Power Amplifier (10F) is a Dual Audio Amplifier IC configured as a 'Bridge Amplifier' and may be either a LM377 or LM378 for Revision A, Audio/Color PCB. Revision letters are locted at position 11C. In later versions of Venture it may possibly use a LM379 with a reconfigured DIP shunt. Information regarding this is available in the operators manual for this game, or contact the Exidy Customer Service Department for assistance if you must use an alternate device.

Volume Controls

Master Volume R46, see the fourth page of Audio/Color PCB schematics.

Music Volume R9, see the fourth page of Audio/Color PCB schematics.

Special Effects Volume R3, see the fourth page of Audio/Color PCB schematics.

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1. Pattern Character Color Division (10A, 9A)

The two segments of Flip-Flop 10A, using the upper two address lines from the character generator circuit, divide the character generator RAM space into four (4) conceptual groups (or quadrants) according to address. This is done in order to assign different colors to different characters.

Using this method, any character stored in a particular quadrant will be the same color as any other character stored in that same quadrant. If the same character is stored in a different quadrant, it will be displayed with a different color. The output of 9A (Two-line to Four-line decoder) applies the separated video lines of these quadrants to priority encoder 10B, whose task is to determine which image is to take visual preference when two or more coincide on the TV screen; that is, which image is to appear to be in the "foreground", and which is to appear to be in the "background".

2. Priority Encoder (10B)

All the video signals generated by the logic PCB are applied to the priority encoder. The signals assigned the higher priority are shown at the top, and the lower priority are shown on the bottom. The output of this device is a 3 Bit code representing the highest priority video line active at that instant. This output code is then sent to the color multiplexers as an address which will select the appropriate color for the imagery generated on that video line. Note that the lowest priority input to the encoder is tied permanently low (active). This insures that when no other video is being generated, there is a background color present, unless of course, the program has selected a background color of black at that time.

3. Color Data Latches (11C, 12C, 13C)

These latches are addressed directly by the Logic PCB microprocessor. Here the microprocessor stores the data that determines which character is what color. This data is then passed to the color selection multiplexers.

4. Color Selection Multiplexers (11B, 12B, 13B)

Each of the three multiplexers controls the video output to a different color gun in the CRT. One turns the red gun on or off, one turns the green gun on or off, and the third does the same for the blue gun. The output combination of the three multiplexers provides for one of eight possible colors to be displayed at any given instant. The color displayed is determined by two things: what type of video is present (e.g. which character), and what color the microprocessor has currently assigned to that type of video. As mentioned above, the color assignations are stored in the color data latches. The priority encoder (10B) issues the code representing the type of video currently displayed. Using these two pieces of information, the multiplexers look at the appropriate bits in the color latches and send the data directly to the TV to turn the color guns on or off.

5. Video and Sync Signal Polarity Selection (11A, 12A)

Before being reclocked one last time, all video outputs are passed through an Exclusive-Or gate (11A), so that one input of each segment can be used to invert the video (make it 180 degrees out of phase with respect to the input to the gate). This feature insures compatibility with TV monitors made by several different manufacturers.

The TV Sync signals are also routed through Exclusive-Or gate segments (12A) for the same purpose.

6. Final Video Output Re-synchronization (13A)

To insure that all video signals and sync signals are accurately synchronized in time, they are all re-clocked one last time together by a HEX "D" Flip-Flop. It "cleans up" any spurious irregularities or propagation delays that may have crept into any of the video or sync signals.

PAGE 1 OF 1: MEMORY EXPANSION PCB

For information on the Memory Expansion PCB, refer to PAGE 5 OF 8, GAME LOGIC PCB. See section 1. Program Memory (6A through 13A)

POWER SUPPLY INFORMATION AND ADJUSTMENTS

All DC Power required to operate VENTURE™ is supplied in the Exidy Power Supply Module. These supply outputs are as follows:

+5v DC	@	6 amps
-5v DC	@	1 amp
+12v DC (HI)*	@	3 amps
+12v DC (HI)*	@	1 amp
-12v DC (HI)*	@	3 amps
-12v DC (LO)*	@	1 amp

* (HI) refers to 'high current'
* (LO) refers to 'low current'

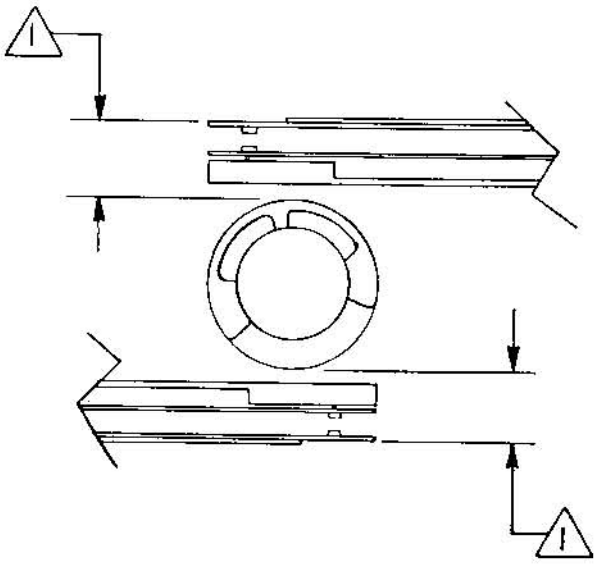
CAUTION: Only certified technicians should make adjustments on all components of VENTURE™. AC line voltage selection is available in your VENTURE™ game by setting the appropriate jumpers on the power chassis. Only the +5v DC is adjustable. This must be adjusted to:

+5.00v DC +/- .25v

as measured on the PCB near the microprocessor (location 2A).

JOYSTICK ADJUSTMENTS

The leaf switches on the 8-position joystick should be adjusted to a dimension of .218" to .250" (7/32" to 1/4"). This is measured from the edge of the joystick shaft to the rear leaf. See the drawing below. Misadjustment will cause the joystick either to activate too soon or to make the 45 degree directions hard to activate.



1 ADJUST TO BE FROM .218 TO .250 FOR IDEAL SWITCH OPERATION.

VENTURE™ AUDIO DIAGNOSTIC TEST

When VENTURE™ is first powered on, the following message appears for eight seconds:

STAND BY

VERSION X

(X= particular version number).

Five seconds after power on, one or more quick beeps, like an organ chord, are heard. This is part of the Exidy Audio Diagnostic Test. The number of beeps that sound indicate different conditions of the Audio board. The following code is an indication **only**, of where to first check the Audio Board. Because this diagnostic test only evaluates certain components, other circuitry is relied upon for the test. Should this other circuitry fail, the diagnostic test may not, then, point directly to the failure. Please use the results of this test as a guideline for further troubleshooting.

The code is as follows:

0 beep: If no beeps are heard, along with a hum or random notes, this may indicate a failure in 3A and/or 7A.

1 beep: All audio hardware is OK. However, be sure to check the Attract Mode Cycle anyway for a possible message to check the Audio Board. In occasional instances, this can occur. The message will further direct you.

2 beeps: ZERO PAGE RAM failure. Check 6532 RAM I.O. Timer Array at location 7B on the board.

3 beeps: (will not occur)

4 beeps: ROM failure

5 beeps: INTERRUPT failure. Check 6532 at location 7B.

In addition, this message appears during the Attract Mode **only** if the Audio Board needs to be checked:

'CHECK AUDIO BOARD'

XX YY

XX and YY in the message are code characters defined as follows:

XX= 01 = ZERO PAGE RAM FAILURE, check 6532

02 = (will not occur)

n3 = ROM FAILURE. Any number in the XX position ending with a 3 (for example, 23, 33, etc.) indicates a ROM failure. The first digit (2 and 3 in the previous example) points you to the appropriate chip that needs to be checked. The code for the any number ending with 3 in the XX position is as follows:

XX=	Chip to Check
03	3A
13	4A
23	5A
33	6A
43	7A

Note: The message reflects the first bad chip it encounters, in numeric order. It is possible for chips following it to also be bad.

04 = INTERRUPT FAILURE, check 6532.

?? = FAULTY COMMUNICATIONS. Check 6520 at 9B.

Here is the code for the second two numbers in the YY position.

YY= 40 = Communication **from** Logic Board **to** Audio failed. Check 6520, both locations 8B and 9B.

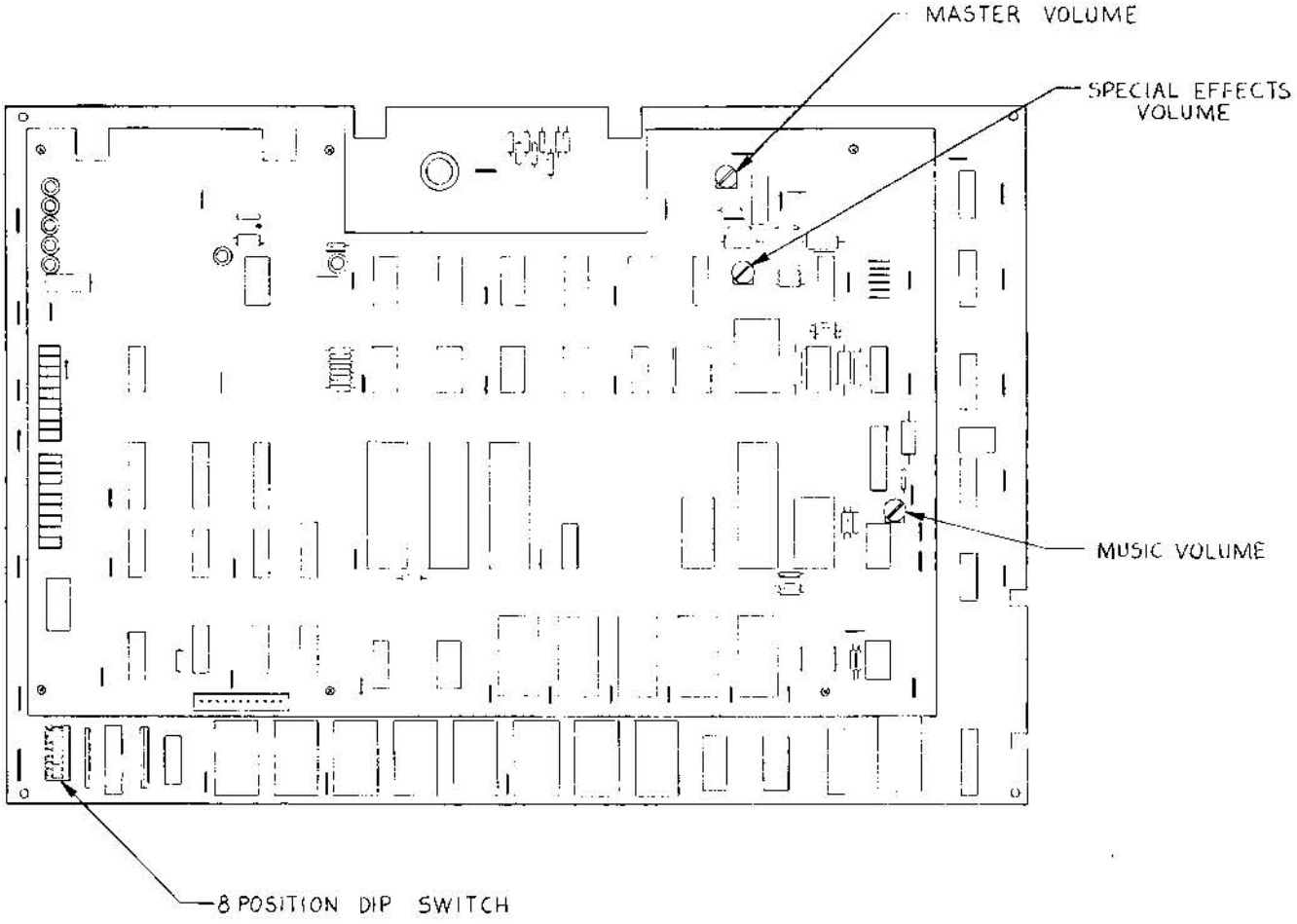
80 = Communication **to** Logic Board **from** Audio failed. Check 6520, at locations 9B and especially 8B.

<0 = Communication between Logic and Audio failed. Check 6520, both locations 8B and 9B.

Also, the symbol <0 in both the XX and YY position, along with a hum or random notes and no beep after power on, may indicate a failure in 3A and/or 7A.

AUDIO BOARD ADJUSTMENTS

The following drawing points out the three individual audio adjustments and the location of the DIP switch. The audio board rides piggyback on the logic board, mounted on the right wall of the game, when viewed from the rear service door.



6.10 LOGIC BOARD, 77-3374-15

Item	Part Number	Description	Location
	77-3374-15	LOGIC BOARD ASSEMBLY 1	
1		LOGIC PRINTED CIRCUIT BOARD	
2	48-2000-11	I.C. 74LS00	3D, 15C, 15H
3	48-2005-11	I.C. 74LS02	1H, 6H, 8F
4	48-2010-11	I.C. 74LS04	1D, 4D, 3F, 10F, 11F
5	48-2015-10	I.C. 7407	2C
6	48-2020-11	I.C. 74LS08	5E
7	48-2332-11	I.C. 74LS11	3H
8	48-2035-11	I.C. 74LS20	2F
9	48-2316-11	I.C. 74LS21	12F, 15E
10	48-2045-11	I.C. 74LS27	7F, 2H
11	48-2055-11	I.C. 74LS32	6F
12	48-2067-11	I.C. 74LS74	1C
13	48-2071-11	I.C. 74LS112	2E, 6E
14	48-2307-11	I.C. 74LS138	5B, 5D
15	48-2321-11	I.C. 74LS139	7E, 16H
16	48-2090-11	I.C. 74LS157	14A, 14E
17	48-2095-11	I.C. 74LS161	1E, 2D, 4F, 5F
18	48-2100-11	I.C. 74LS166	12B, 12D, 13D, 14D, 15D
19	48-2115-11	I.C. 74LS193	10E, 12E, 13F, 15F, 14F, 16F, 11E 13E
20	48-2328-11	I.C. 74LS241	1A, 3A, 15A, 3B, 6B, 9B, 8C, 7D, 9E, 4H
21	48-2350-11	I.C. 74LS245	3C, 4C, 6C, 13B, 15B
22	48-2314-11	I.C. 74LS374	1F, 14B, 7C, 9D, 8E
23	48-6502	MICROPROCESSOR 6502	2A
24	48-2334	2114 RAM (1K x 4)	4A, 5A, 7B, 8B, 11C, 12C, 13C, 14C
25	48-9219	6301 PROM (256x4) VEL5C-1	5C
26	48-9099-01	6331 PROM (32x8) HRL6D-1	6D
27	48-9099-02	6331 PROM (32x8) HRL14H-1	14H
28	46-3025	1N4002 DIODE	8E, 9F, 2H
29	49-5135	RES. 470 OHM 1/4W 5%	1D, 2H
30	59-5120	RES. 1.2K 1/4W 5%	2C
31	59-5115	RES. 1.8K 1/4W 5%	1C, 2C
32	59-5110	RES. 2.2K 1/4W 5%	7E, 2A
33	59-5105	RES. 2.7K 1/4W 5%	1C, 2C
34	51-0003	RES. 220 OHM 1/8W 5% 10 Pin Sip	9E
35	51-0002	RES. 2.2K 1/8W 5% 10 Pin Sip	16A
36	51-0001	RES. 4.7K 1/8W 5% 10 Pin Sip	15A
37	51-0004	RES. 6.8K 1/8W 5% 10 Pin Sip	14A
38	23-4033	CAP. .01uf CERAMIC DISC	1D
39	23-4035	CAP. .1uf CERAMIC DISC	A/R

LOGIC BOARD, continued

Item	Part Number	Description	Location
40	21-4015	CAP. 6.8uf 25v DIPTANT	1C, 15D, 6E, 13F
41	20-4014	CAP. 33uf 25V ELECTROLYTIC	1C, 2C
42	20-4005	CAP. 470uf 10V ELECTROLYTIC	10H
43	72-3025	DIPSHUNT JUMPER PAKS 16 PIN	4B, 11B, 10D
44	72-3042	DIP SWITCH 8 POS.	16A
45	45-3036	CRYSTAL 11.289mhz (SERIES)	1D
46	61-8041	CONN. 10 PIN MOLEX	16C, 16F
47	61-8062	DIP SOCKETS 16 PIN LOW PROFILE	4B, 11B, 5C, 6D 14H, 10D
48	61-8045	DIP SOCKETS 24 PIN LOW PROFILE	6A thru 13A, 11D
49	61-8035	DIP SOCKETS 40 PIN LOW PROFILE	2A
50	61-8060	DIP SOCKETS 14 PIN LOW PROFILE	16B
51	61-8157	DIP SOCKETS 18 PIN LOW PROFLE	4A, 5A, 7B, 8B, 11C 12C, 13C, 14C
52	21-4021	CAP 1uf 25V DIP TANT	C45 thru C52, 5D, 2H
53	59-5138	RES. 220 OHM 1/4W 5%	R200, R311
54	59-5179	RES. 18 OHM 1/4W 5%	R300 thru R302
55	23-4067	CAP. 330 pf CER. DISC	5D
56	48-9224	E PROM, 2732 VEL6A-1	6A
57	48-9225	E PROM, 2732 VEL7A-1	7A
58	48-9226	E PROM, 2732 VEL8A-1	8A
59	48-9227	E PROM, 2732 VEL9A-1	9A
60	48-9228	E PROM, 2732 VEL10A-1	10A
61	48-9229	E PROM, 2732 VEL11A-1	11A
62	48-9230	E PROM, 2732 VEL12A-1	12A
63	48-9231	E PROM, 2732 VEL13A-1	13A
64	48-9220	E PROM, 2716 VEL11D-1	11D

6.11 AUDIO/COLOR BOARD ASSEMBLY 77-3386-15

1		PRINTED CIRCUIT BOARD	
2	48-2307-11	I.C. 74LS138	13D
3	48-6520	I.C. 6520	8B, 9B
4	48-9209	I.C. 6532	7B
5	48-6502	I.C. 6502	3B
6	48-9210	I.C. 6840	3D
7	48-9211-11	I.C. 74LS154	4B
8	48-9212	I.C. 8253	2B
9	48-9213	I.C. 4069	1A
10	48-9069	I.C. 4013B	1B

AUDIO/COLOR BOARD ASSEMBLY, continued

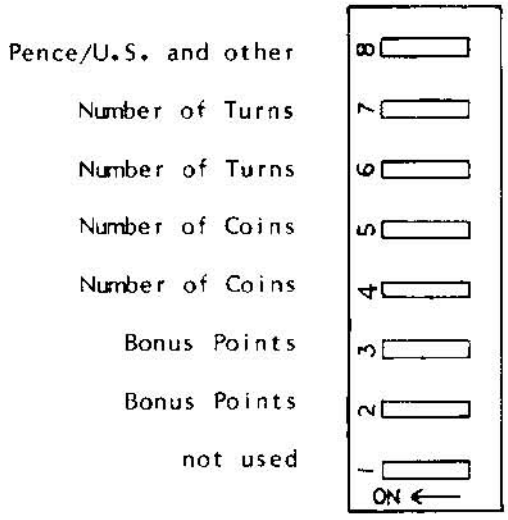
Item	Part Number	Description	Location
11	48-2010-11	I.C. 74LS04	5D
12	48-2000-11	I.C. 74LS00	6B
13	48-2314-11	I.C. 74LS374	1C, 11C, 12C, 13C
14	48-9214	I.C. 4053	2D, 4D
15	48-9215	I.C. 4175	6E, 73, 8E, 9E
16	48-9216	I.C. 4562	5E
17	48-2067-11	I.C. 74LS74	10A, 6D
18	48-2342	I.C. LM324	3F, 2E
19	48-2013-10	I.C. 7406	1D
20	48-2341-11	I.C. 74LS86	11A, 12A, 4E
21	48-9217	I.C. 4051	7D, 8D, 9D
22	48-2321-11	I.C. 74LS139	9A
23	48-9112	I.C. LM377	10E
24	48-2079-11	I.C. 74LS148	10B
25	48-2080-11	I.C. 74LS151	11B, 12B, 13B
26	48-2333-11	I.C. 74LS174	13A
27	48-4035	.1 uf. CERAMIC CAP 25v	1A thru 7A, 9A, 11A, 13A, 1B, 6B, 9B, 11B, 1C, 11C, 13C, 1D 3D, 5D, 7D, 9D, 11D, 13D, 1E, 2E, C7, C9, C10, 3E, 5E, 7E, 9E, C12, 13E, 2F, 4F, 12F, 9E, 2E, 3F
28	23-4070	22pf CERAMIC CAP 16V	C1
29	23-4033	.01 uf CERAMIC CAP 16V	C6, C8, C11, C33, 1C
30	20-4030	33uf CAP, 25V, ELECTROLYTIC W/AXIAL LEADS	C13, C15, C17 thru C21
31	20-4006	100uf CAP ELECTRO-LYTIC 16V	C16
32	20-4009	4.7uf CAP ELECTRO-LYTIC 16V	C3, C4, C5
33	20-4022	1.0uf CAP ELECTRO-LYTIC 16V	C27, C32, C2
34	59-5115	1.8K RES. 1/4W 5%	R3, R4, R5
35	59-5100	3.3K RES. 1/4W 5%	R6
36	59-5125	1K RES. 1/4W 5%	R14
37	59-5016	10M RES. 1/4W 5%	R2
38	59-5182	300 OHM RES. 1/4W 5%	R1
39	59-5045	100K RES. 1/4W 5%	R10, R11, R12, R27 R47, 428, R29
40	59-5070	22K RES. 1/4W 5%	R15, R30
41	59-5025	1M RES. 1/4W 5%	R32 R33, R35
42	59-5065	33K RES. 1/4W 5%	R34
43	59-5105	2.7K RES. 1/4W 5%	R21
44	59-5063	27K RES. 1/4W 5%	R44
45	59-5119	1.3K RES. 1/4W 5%	R26
46	59-5130	680 OHM RES. 1/4W 5%	R19
47	59-5136	330 OHM RES. 1/4W 5%	R7, R8, R24
48	59-5184	160 OHM RES. 1/4W 5%	R25

AUDIO/COLOR BOARD ASSEMBLY, continued

Item	Part Number	Description	Location
49	59-5185	82 OHM RES. 1/4W 5%	R20
50	59-5186	39 OHM RES. 1/4W 5%	R22, R23
51	59-5080	10K RES. 1/4W 5%	R16, R17, R18, R42, R45
52	54-5019	10K POT	R9, R31, R46
53	51-0001	4.7K RES. PAC 10 PIN SIP	4D
54	45-3048	3.579545 MHZ CRYSTAL	2A
55	72-3025	16 PIN DIP SHUNT	8A, 11E
56	61-8060	14 PIN DIP SOCKET	J20, 1A, 1B, 5E
57	61-8045	24 PIN DIP SOCKET	3A, 4A, 5A, 6A, 7A, 2B
58	61-8103	28 PIN DIP SOCKET	3D
59	61-8035	40 PIN DIP SOCKET	3B, 7B, 8B, 9B
60	61-8062	16 PIN DIP SOCKET	2D, 4D, 8A, 11E, 6E- 9E, 7D-9D
61	22-4025	.47 uf CAP ELECTRO-LYTIC 16V	C14
62	61-8203	10 PIN MALE CONNECTOR	P21
63	61-8042	10 PIN FEMALE CON-NECTOR	J2, J3
64	68-0071	HEATSINK STAVER V7-1	ONLY W/ LM277, LM278
65	48-9232	E PROM 2716, VEA3A-1	3A
66	48-9233	E PROM 2716, VEA4A-1	4A
67	48-9233	E PROM 2716, VEA5A-1	5A
68	48-9235	E PROM 2716, VEA6A-1	6A
69	48-9236	E PROM 2716, VEA7A-1	7A

SELECTABLE OPTIONS

VENTURE™ has several switch selectable options controlled by an 8-position DIP switch located on the main logic board at position 16A. This switch is accessible through the back door of the game. The previous drawing shows the location of the DIP switch. The following drawing shows the particular functions controlled by the 8- position DIP switch.



Functions of the 8- position DIP Switch

5.1 Selectable Dip Switch Settings

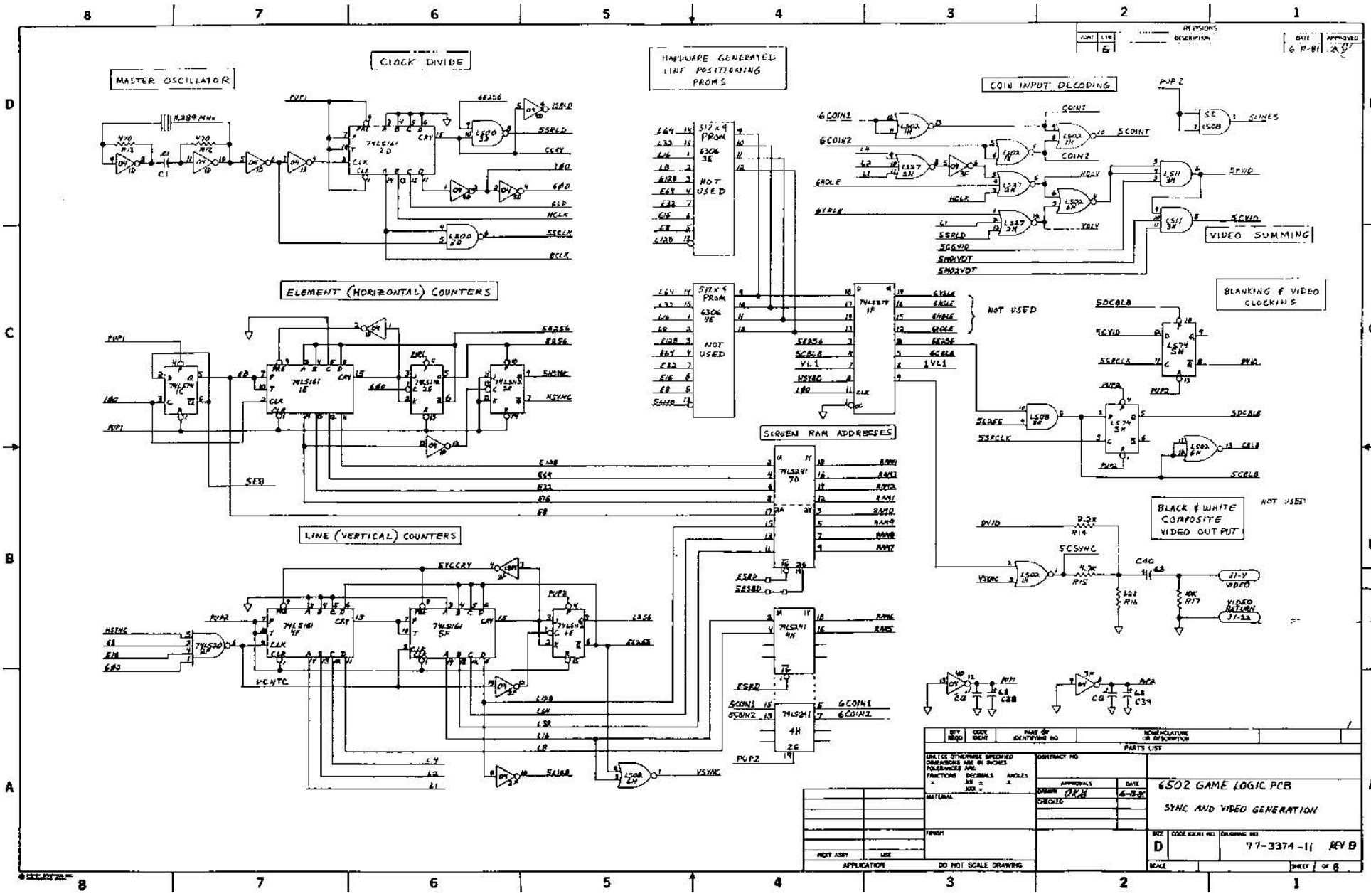
VENTURE™ is shipped with the dip switch already set for optimum dollar return. Should you decide to change the settings, you may select any of the following options by setting the proper switch accordingly:

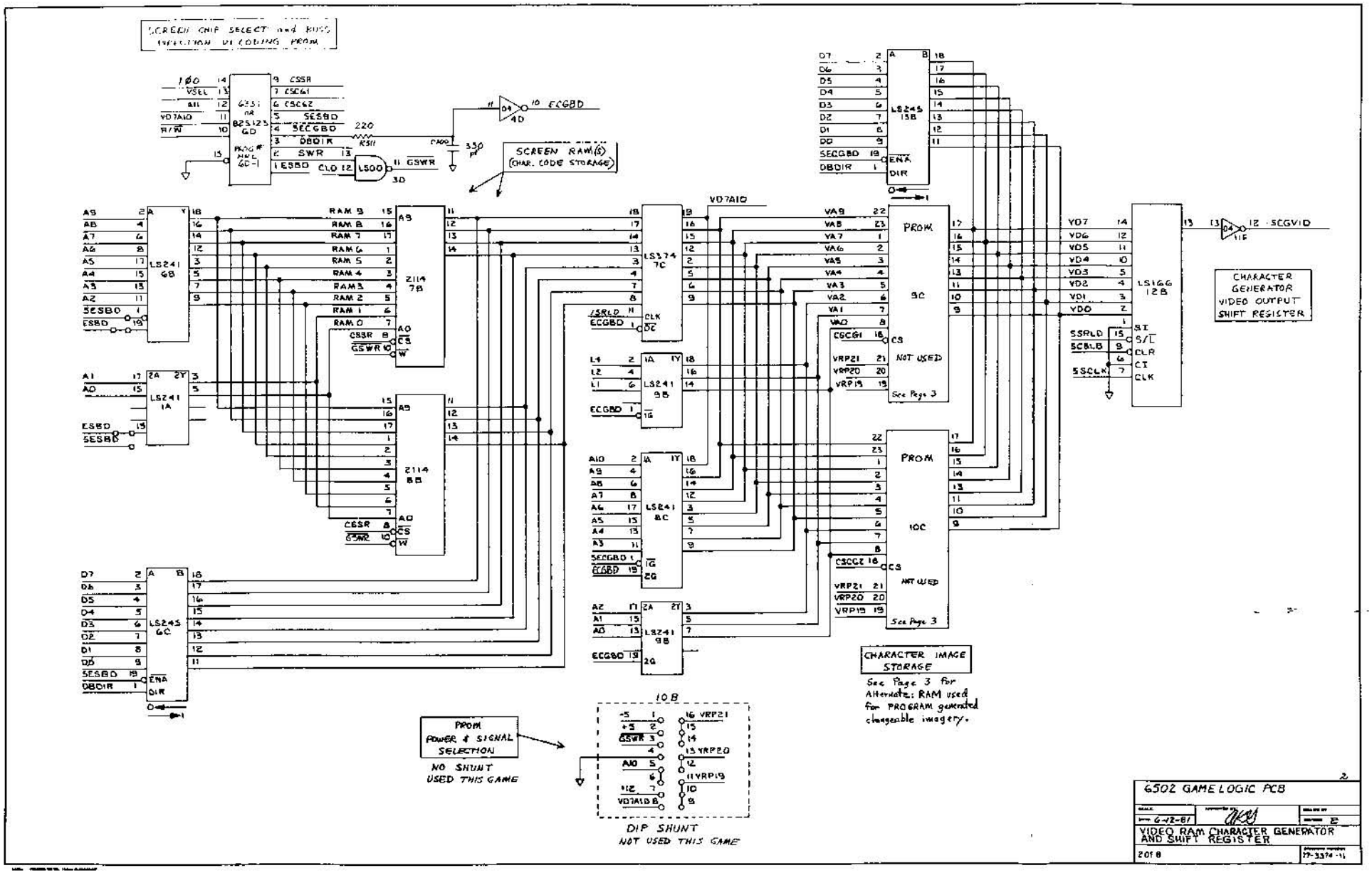
A. COINAGE	Switch 4	Switch 5	Switch 8
2 Plays - 1 Coin	OFF	OFF	OFF
1 Play - 1 Coin 2 Plays - 2 Coin	ON	OFF	OFF
1 Play - 2 Coin 2 Plays - 4 Coin	OFF	ON	OFF
1 Play - 20 pence 3 Plays - 50 pence	ON	ON	ON

B. TYPE OF COINS	Switch 8
U.S. and other	OFF
English coins	ON

D. NUMBER OF TURNS	Switch 6	Switch 7
2 Bows and arrows (turns)	ON	ON
3 Bows and arrows	OFF	ON
4 Bows and arrows	ON	OFF
5 Bows and arrows	OFF	OFF

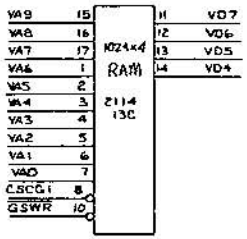
E. BONUS BOW (Extra turn awarded when selectable number of points are made).	Switch 2	Switch 3
Extra turn for 20,000 points	ON	ON
30,000	OFF	ON
40,000	ON	OFF
50,000	OFF	OFF

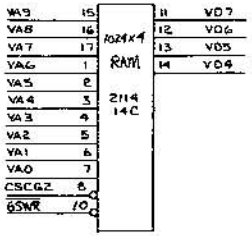

MASTER OSCILLATOR
CLOCK DIVIDE
HARDWARE GENERATED LINE POSITIONING PROMS
COIN INPUT DECODING
VIDEO SUMMING
ELEMENT (HORIZONTAL) COUNTERS
SCREEN RAM ADDRESSES
BLANKING & VIDEO CLOCKING
LINE (VERTICAL) COUNTERS
BLACK & WHITE COMPOSITE VIDEO OUT PUT
NOT USED
6502 GAME LOGIC PCB
SYNC AND VIDEO GENERATION
77-3374-11
REV B
DO NOT SCALE DRAWING

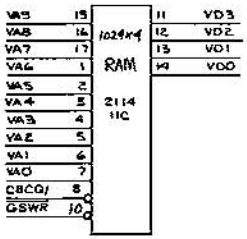

SCREEN CHIP SELECT and BUS INJECTION DECODING PROM
SCREEN RAM(S) (CHAR. CODE STORAGE)
CHARACTER GENERATOR VIDEO OUTPUT SHIFT REGISTER
CHARACTER IMAGE STORAGE
See Page 3 for Alternate: RAM used for PROGRAM generated changeable imagery.
PROM POWER & SIGNAL SELECTION
NO SHUNT USED THIS GAME
DIP SHUNT
NOT USED THIS GAME
6502 GAME LOGIC PCB
VIDEO RAM CHARACTER GENERATOR AND SHIFT REGISTER
2018
2
6-12-81

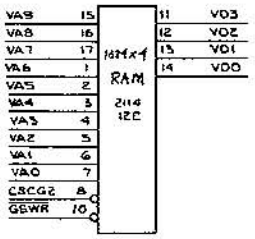
CHARACTER GENERATOR
IMAGE STORAGE RAMS

For use with PROGRAM
generated changeable imagery.









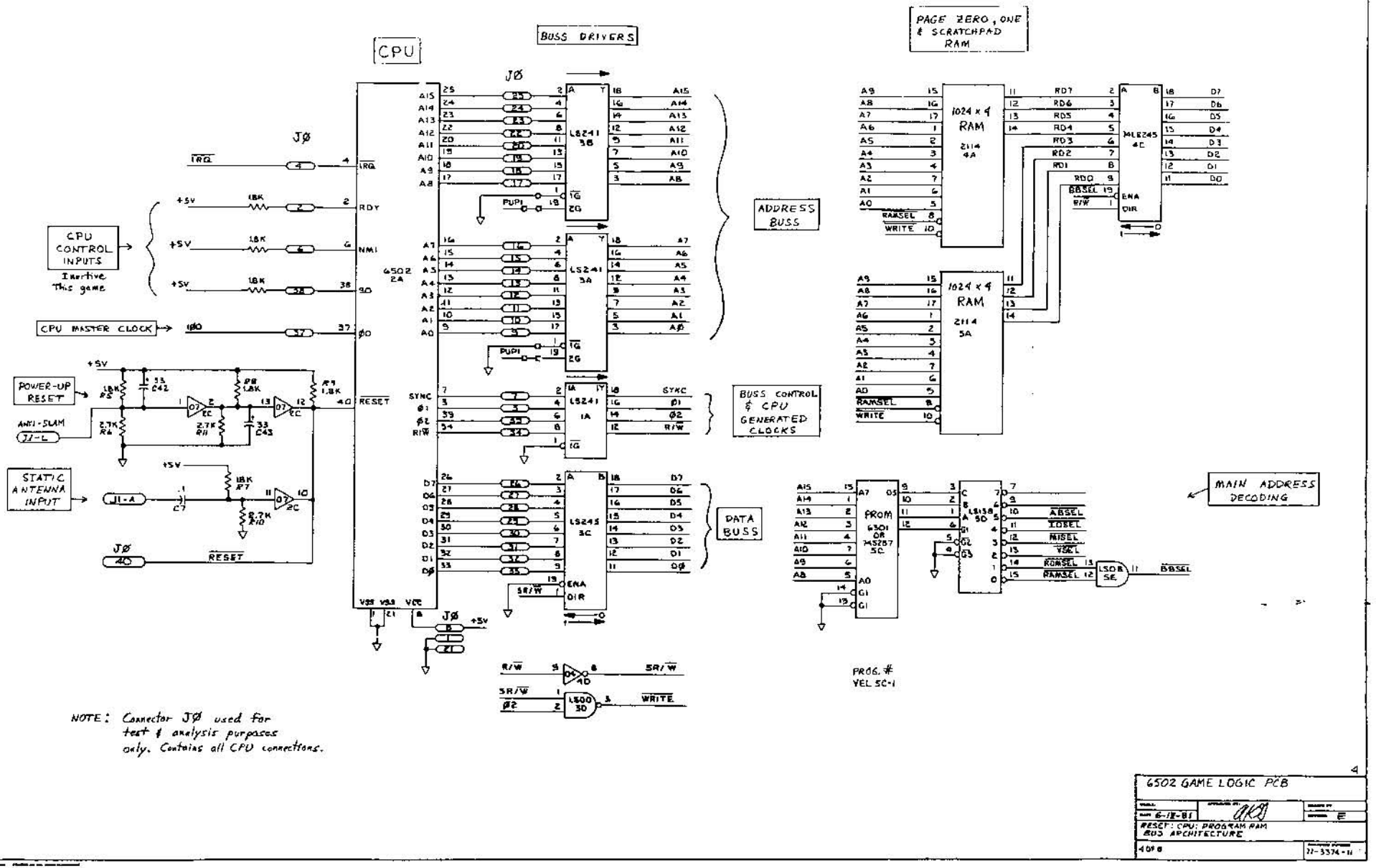
3

6502 GAME LOGIC PCB

	AKB	
DATE 6-12-81		DRAWN BY G

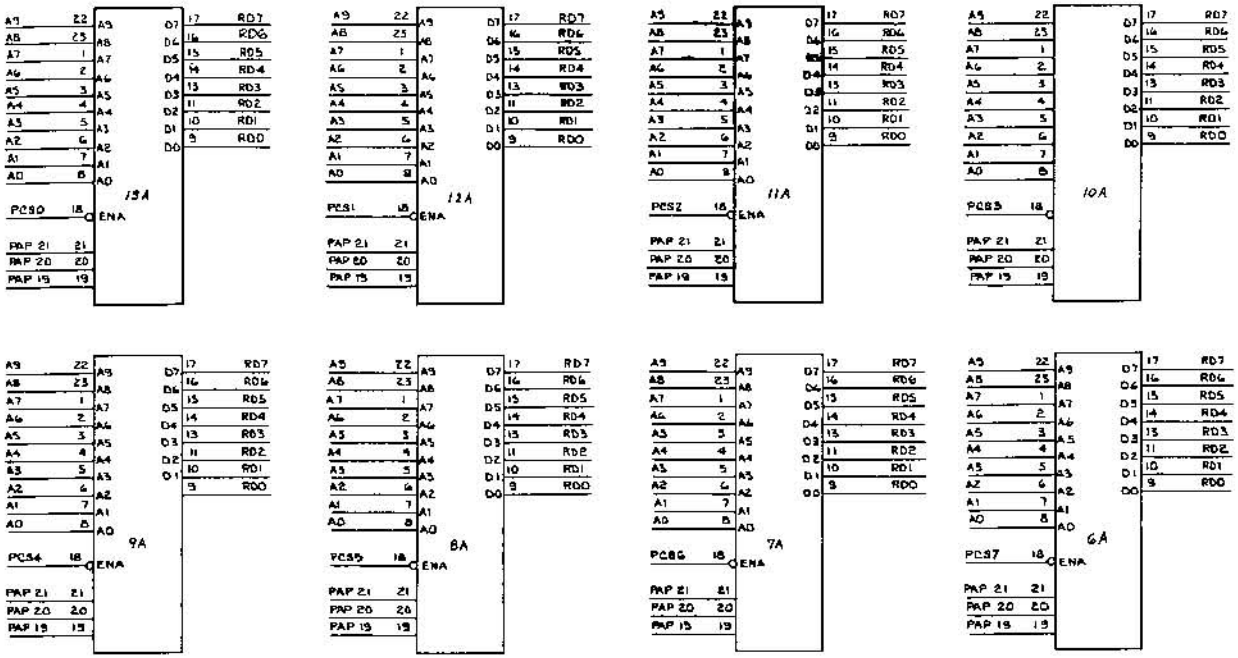
IMAGE STORAGE RAM

9 OF 9	23-3574-13


CPU
BUSS DRIVERS
PAGE ZERO, ONE & SCRATCHPAD RAM
JØ
IRQ
+5V
1BK
RDY
NMI
SO
CPU CONTROL INPUTS
Inactive This game
CPU MASTER CLOCK
1Ø
ØO
RESET
POWER-UP RESET
ANTI-SLAM
J1-L
STATIC ANTENNA INPUT
J1-A
6502 2A
LS241 3B
LS241 3A
LS241 1A
LS245 3C
ADDRESS BUSS
BUSS CONTROL & CPU GENERATED CLOCKS
DATA BUSS
1024 x 4 RAM 2114 4A
1024 x 4 RAM 2114 5A
74LS245 4C
RAMSEL
WRITE
BBSEL
R/W
ENA
DIR
PROM 6301 OR 745287 5C
LS138 5D
LS08 5E
ABSEL
IOSEL
MISEL
VSEL
ROMSEL
MAIN ADDRESS DECODING
LS00 3D
SR/W
WRITE
PROG. # YEL 5C-1
NOTE: Connector JØ used for test & analysis purposes only. Contains all CPU connections.
6502 GAME LOGIC PCB
6-12-81
AKJ
RESET: CPU: PROGRAM RAM BUS ARCHITECTURE
4 OF 8
21-5374-11

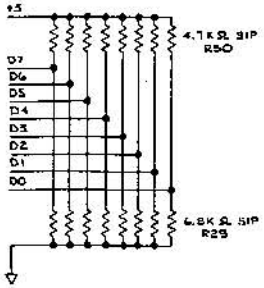
PROGRAM MEMORY

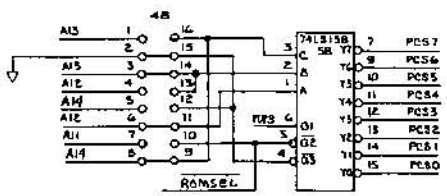
See TECHNICAL MANUAL For PROGRAM #'S.



DATA BUSS TERMINATION

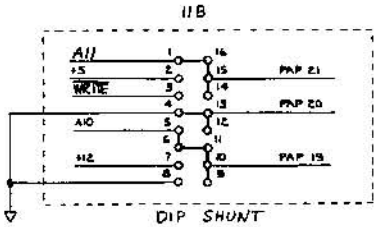
Ringing Suppression





PROM ADDRESS SELECTION

Configuration Shown is for +5V ONLY 2732 EPROMS. See TECHNICAL MANUAL For configuration for other memory devices.



DIP SHUNT

MEMORY DEVICE PERSONALITY SELECTION

Configuration shown is for +5V ONLY 2732 EPROMS. See TECHNICAL MANUAL for configuration for other memory devices.

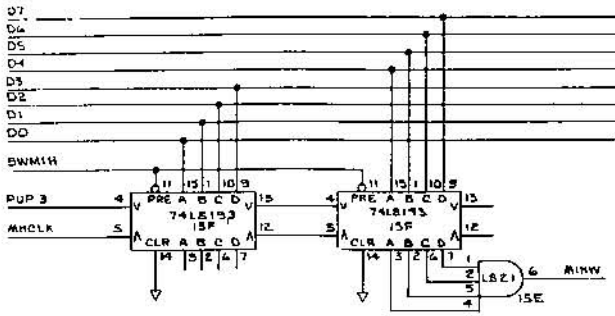
EXIDY INC.

6502 GAME LOGIC PCB
CPU ROM

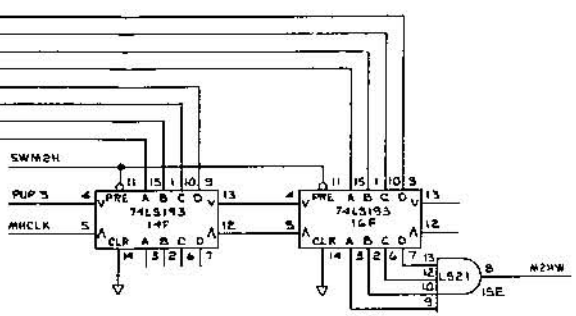
5 OF 8

5

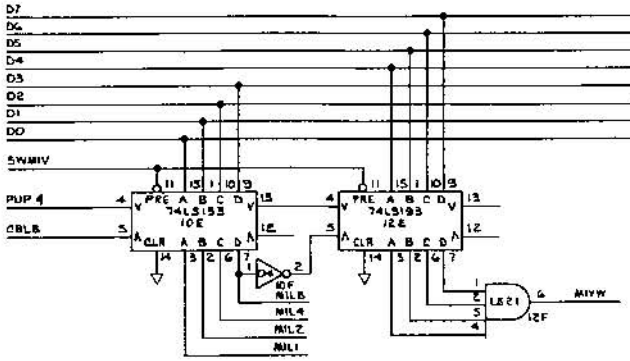
MOVING OBJECT 1
HORZ. COUNTERS



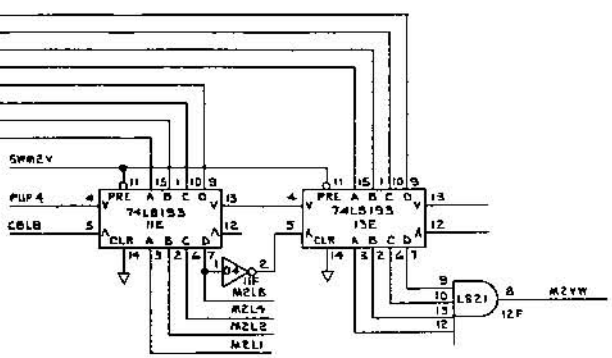
MOVING OBJECT 2
HORZ. COUNTERS

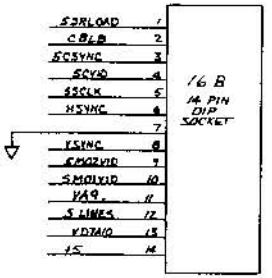


MOVING OBJECT 1
VERTICAL COUNTERS

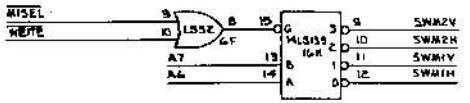


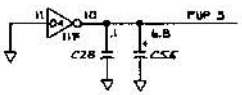
MOVING OBJECT 2
VERTICAL COUNTERS

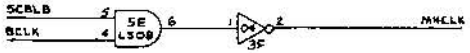




VIDEO
OUTPUT
TO
AUDIO/COLOR PCB







'WRITE MOVING OBJECT' DECODING

6

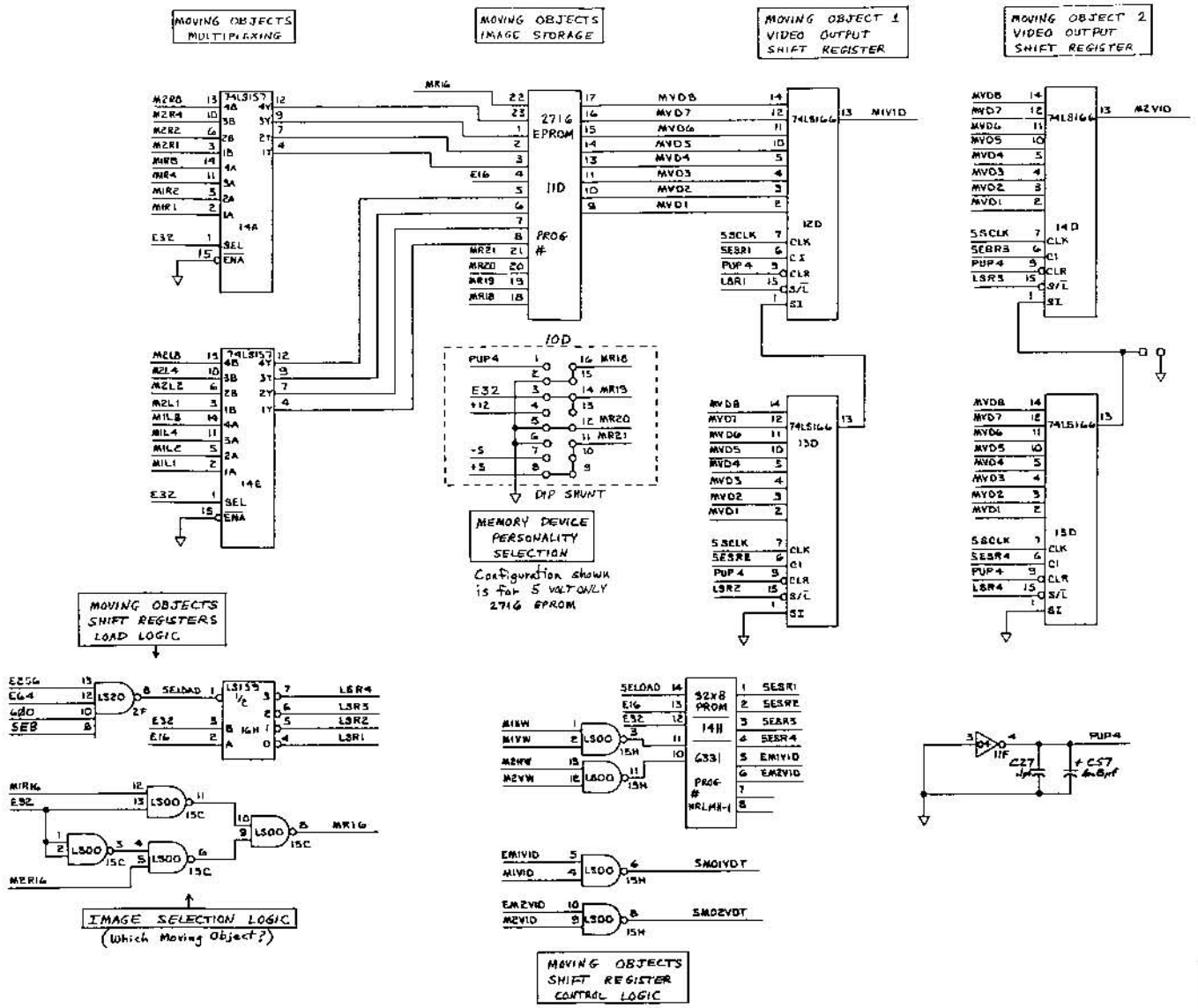
G502 GAME LOGIC PCB

SCALE	APPROVED BY	DRAWN BY
DATE 6-12-81	AKB	REVISION B

COLOR INTERFACE OUTPUT AND MOVING OBJECT POSITION COUNTERS

6 OF 8

DRAWING NO. 77-3534-11



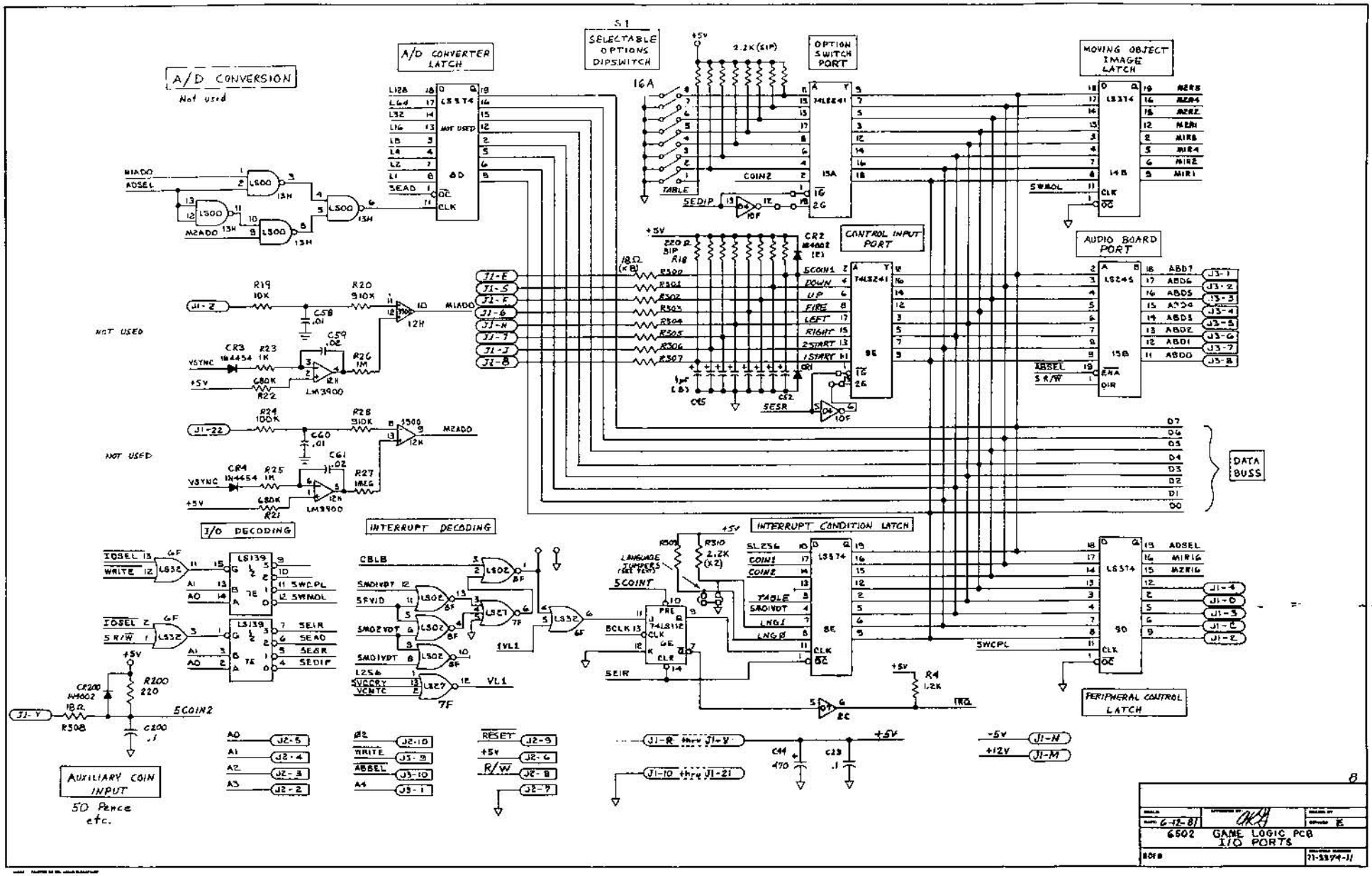
7

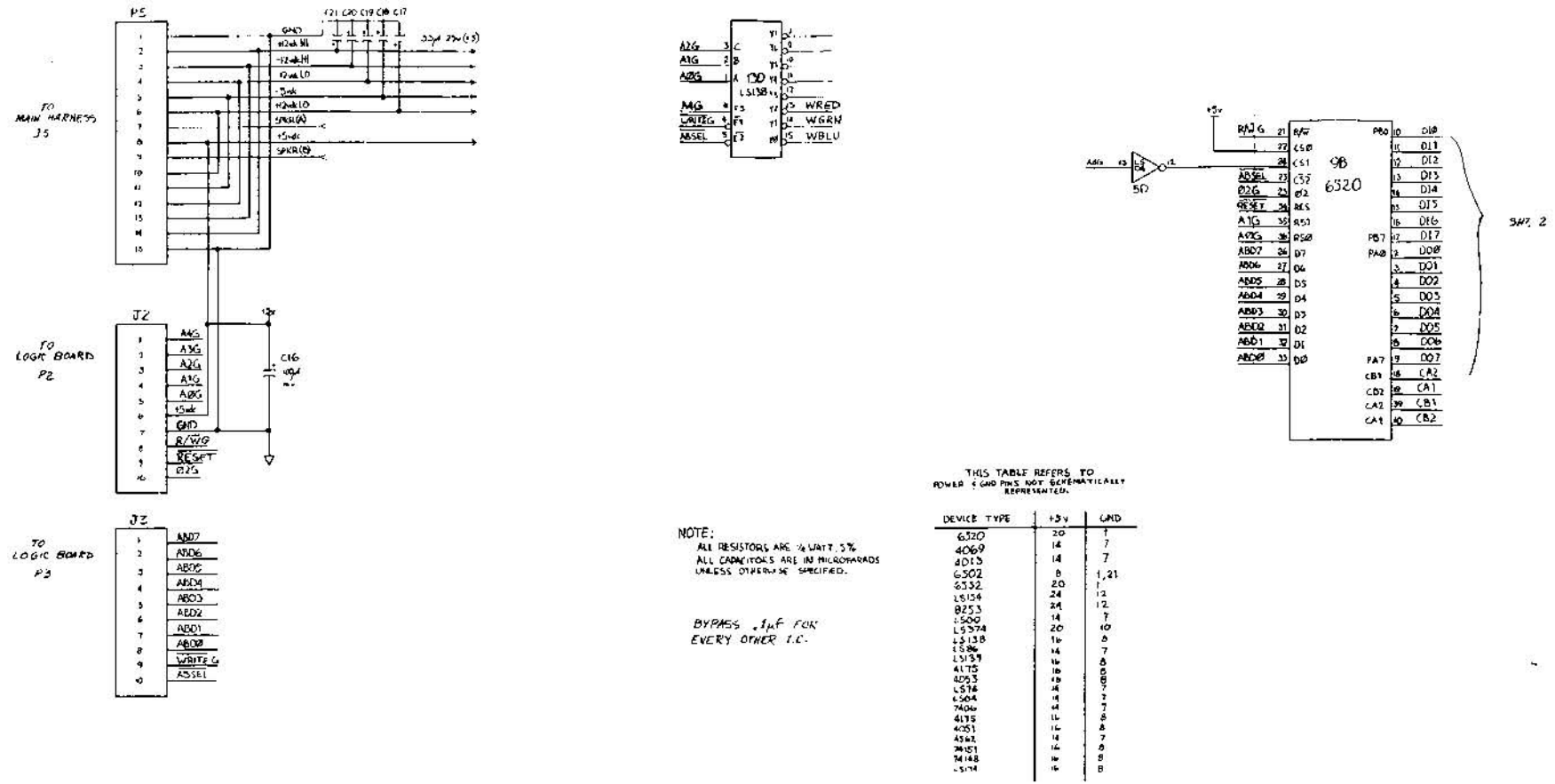
6502 GAME LOGIC PCB

MOVING OBJECT VIDEO GENERATION

8 OF 8

21-5126-11


A/D CONVERSION
Not used
A/D CONVERTER LATCH
SELECTABLE OPTIONS DIPSWITCH
S1
16A
OPTION SWITCH PORT
MOVING OBJECT IMAGE LATCH
CONTROL INPUT PORT
AUDIO BOARD PORT
DATA BUSS
I/O DECODING
INTERRUPT DECODING
INTERRUPT CONDITION LATCH
PERIPHERAL CONTROL LATCH
AUXILIARY COIN INPUT
50 Pence etc.
6502 GAME LOGIC PCB I/O PORTS
6-12-81
21-13174-11



NOTE:
ALL RESISTORS ARE ¼ WATT, 5%
ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

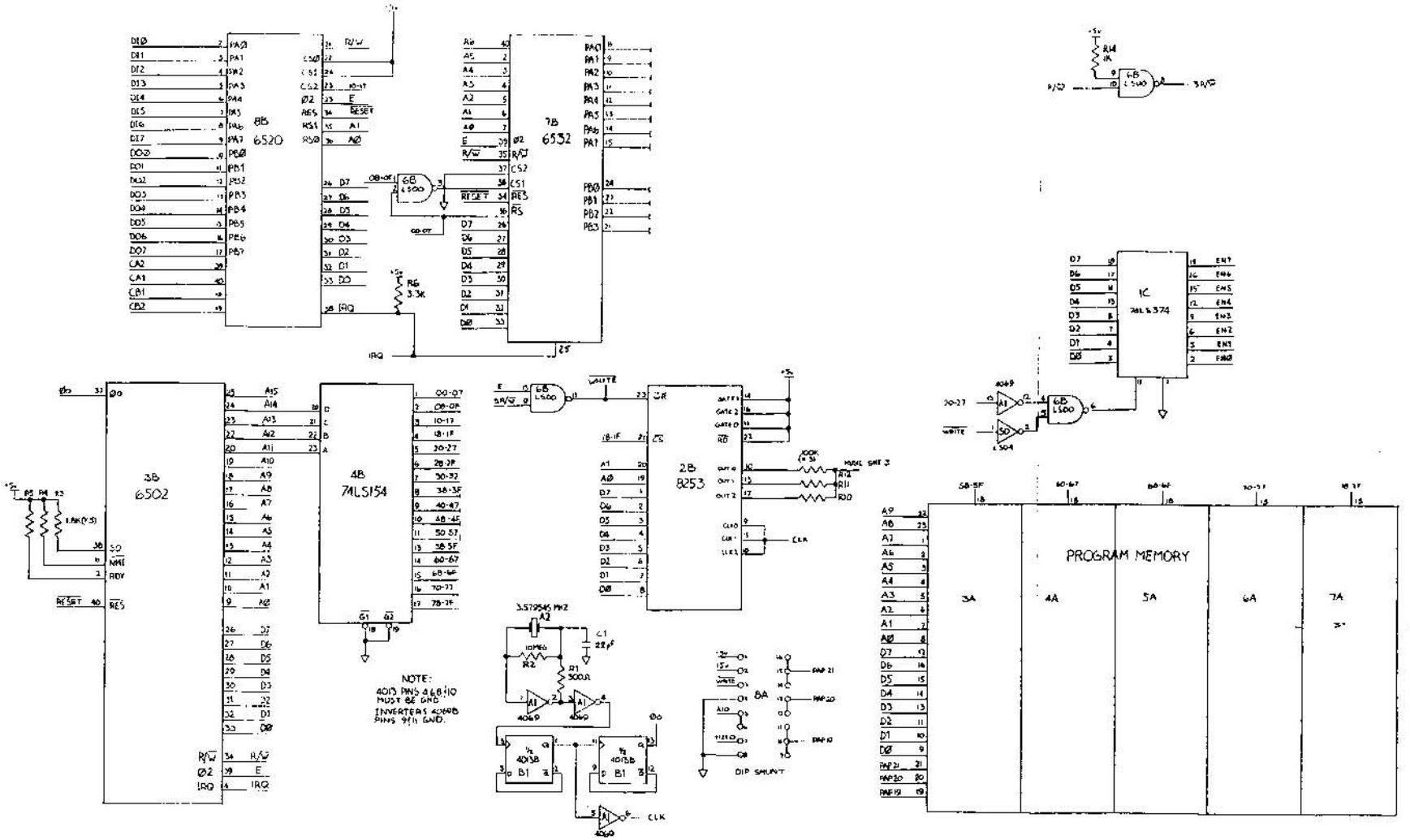
BYPASS .1μF FOR EVERY OTHER I.C.

THIS TABLE REFERS TO POWER & GND PINS NOT SCHEMATICALLY REPRESENTED.

DEVICE TYPE	+5V	GND
6520	20	1
4069	14	7
4013	14	7
6502	8	1,21
6532	20	1
LS154	24	12
8253	24	12
LS09	14	7
LS374	20	10
LS138	16	8
LS86	14	7
LS139	16	8
4LT5	16	8
4053	16	8
LS74	14	7
6504	14	7
7406	14	7
4LT5	16	8
4051	16	8
4562	14	7
74151	16	8
74148	16	8
LS174	16	8

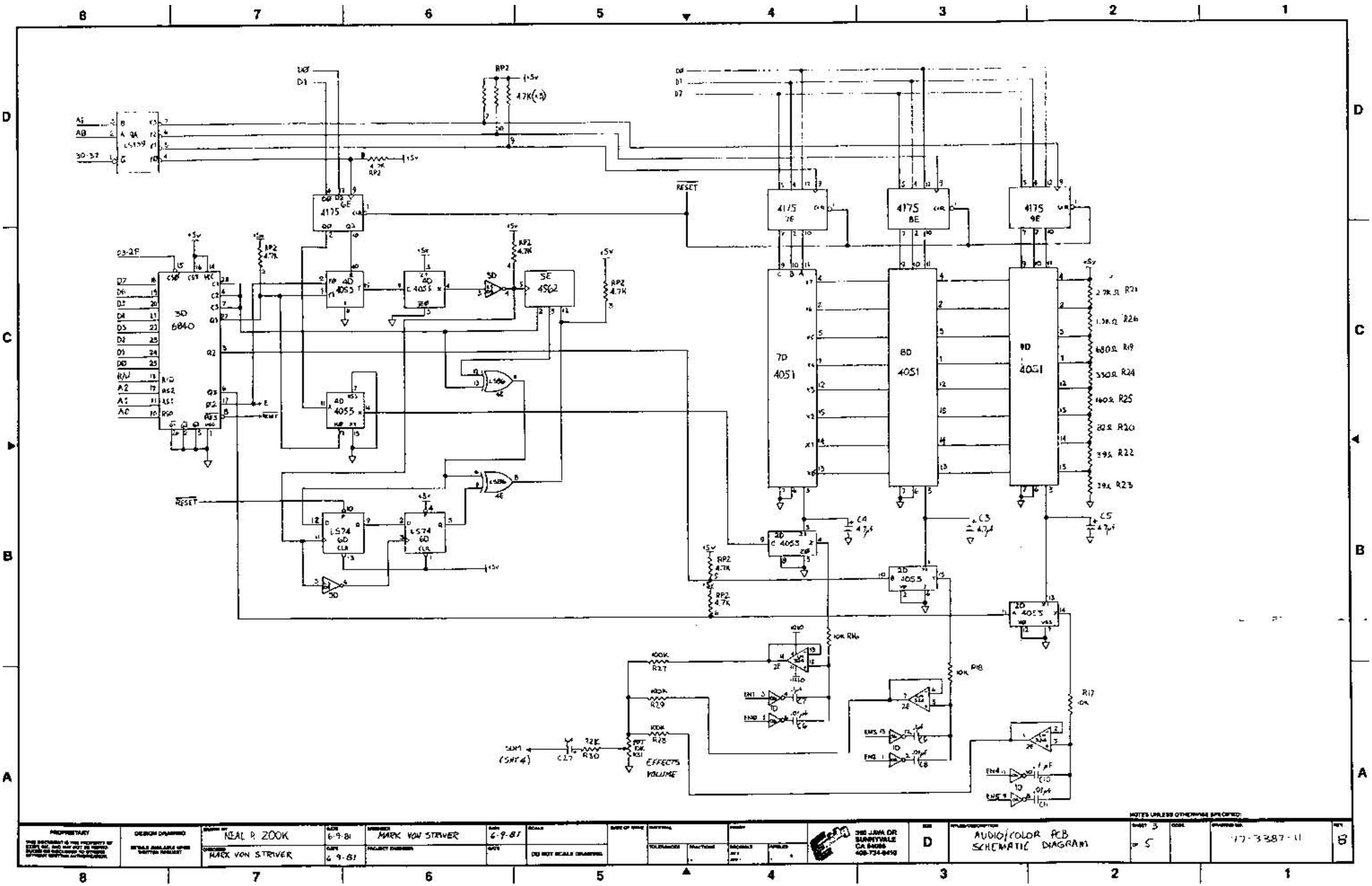
PROPRIETARY	DESIGN DRAWING	DRAWN BY NEAL R. ZOOK	DATE 6-8-81	ENGINEER MARK VON STRIVER	DATE 6-8-81	SCALE DO NOT SCALE DRAWING	DATE OF ISSUE	MATERIAL	FINISH	380 JAVA DR SUNNYVALE CA 94086 408-734-8410	SIZE D	TITLE/DESCRIPTION AUDIO/COLOR PCB SCHEMATIC DIAGRAM	NOTES UNLESS OTHERWISE SPECIFIED: SHEET 1 OF 5	CODE	DRAWING NO. 77-3387-11	REV B
		CHECKED MARK VON STRIVER	DATE 6-8-81	PROJECT ENGINEER												

8 7 6 5 4 3 2 1

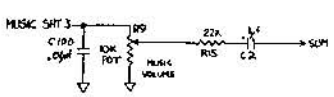


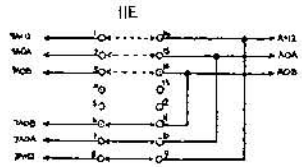
PROPRIETARY	DESIGN DRAWING	DRAWN BY NEAL R ZOOK	DATE 6-5-81	ENGINEER MARK VON STRIVER	DATE 6-6-81	SCALE DO NOT SCALE DRAWING	DATE OF ISSUE	MATERIAL	FINISH	ATARI 330 JAVA DR SUNNYVALE CA 94086 408-734-8400	SIZE D	TITLE/DESCRIPTION AUDIO/COLOR PCB SCHEMATIC DIAGRAM	SHEET 2 OF 5	CODE	DRAWING NO. 77-3387-11	REV B
		CHECKED MARK VON STRIVER	DATE 6-6-81	PROJECT ENGINEER	DATE			TOLERANCES FRACTIONS								

NOTES UNLESS OTHERWISE SPECIFIED: 12

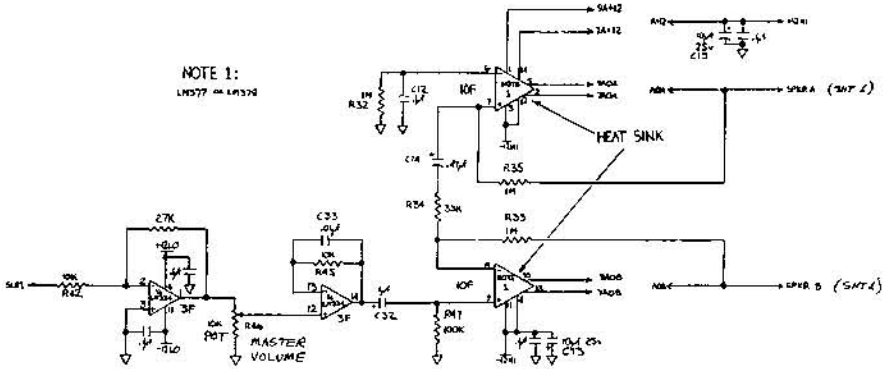


4175 6E
4175 7E
4175 8E
4175 9E
LS139
3D 6840
4D 4053
4D 4055
5E 4562
LS86 4E
LS74 6D
7D 4051
8D 4051
9D 4051
2D 4053
2D 4055
RESET
2.7K Ω R21
1.5K Ω R26
680 Ω R19
330 Ω R24
160 Ω R25
82 Ω R20
39 Ω R22
39 Ω R23
SUM (SHT 4)
EFFECTS VOLUME
PROPRIETARY
DESIGN DRAWING
NEAL P. ZOOK 6-9-81
MARK VON STRIVER 6-9-81
MARK VON STRIVER 6-9-81
DO NOT SCALE DRAWING
NOTES UNLESS OTHERWISE SPECIFIED:
390 JAVA DR SUNNYVALE CA 94086 408-734-8410
D
AUDIO/COLOR PCB SCHEMATIC DIAGRAM
SHEET 3 OF 5
17-3387-11
B



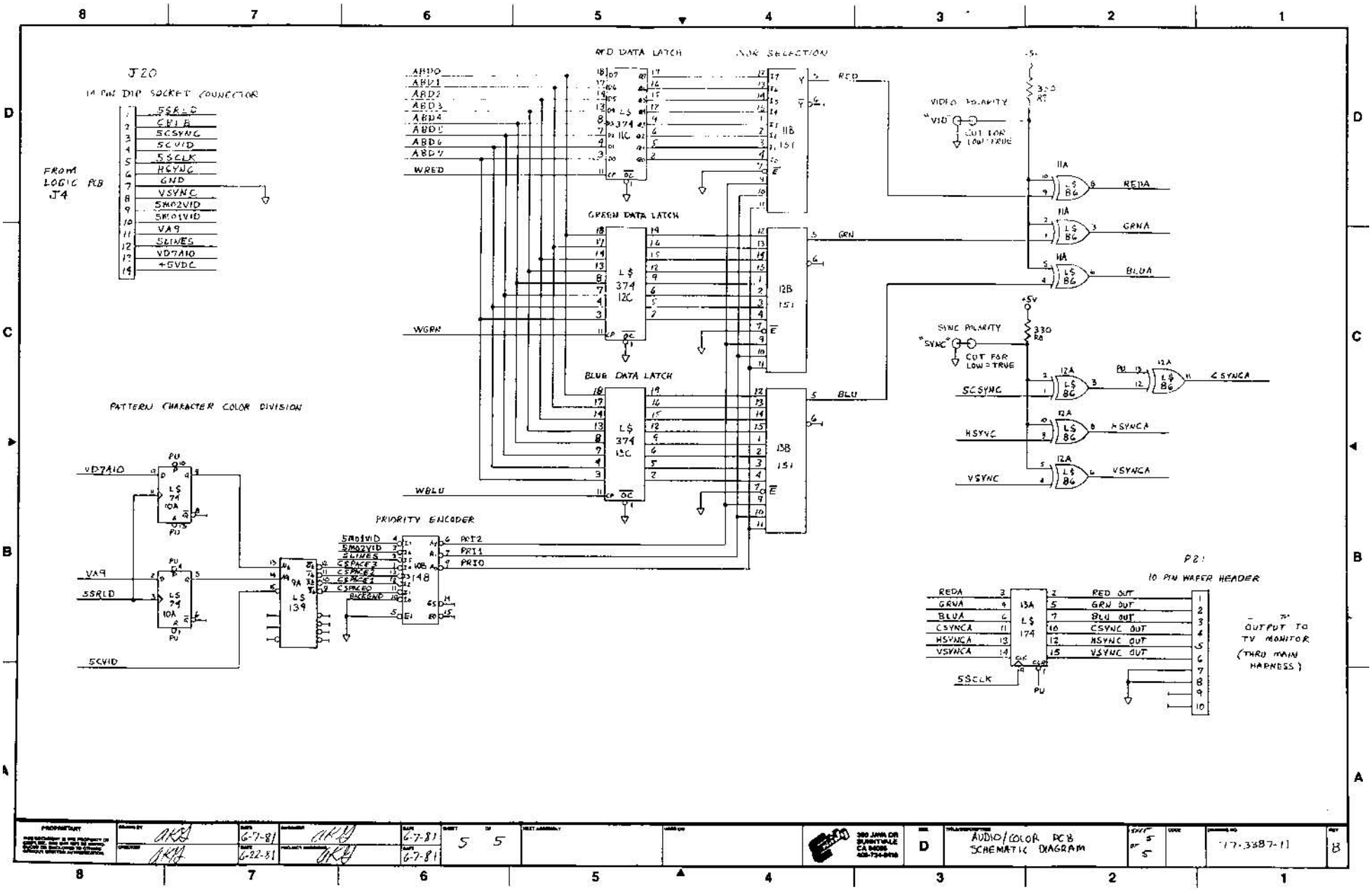


NOTE 1:
LM377 OR LM378



PROPRIETARY	DESIGN DRAWING	DRAWN BY NEAL R. ZOOK	DATE 6-9-81	CHECKED MARK VON STRIVER	DATE 6-9-81	SCALE DO NOT SCALE DRAWING	SIZE OF ISSUE	MATERIAL		FINISH		350 JAVA DR SUNNYVALE CA 94086 408-734-8496	SIZE D	TITLE/DESCRIPTION AUDIO/COLOR PCB SCHEMATIC DIAGRAM	SHEET 4 OF 5	CODE	DRAWING NO. 77-3387-11	REV. 8
		CHECKED MARK VON STRIVER	DATE 6-9-81	PROJECT ENGINEER	DATE												

NOTES UNLESS OTHERWISE SPECIFIED:

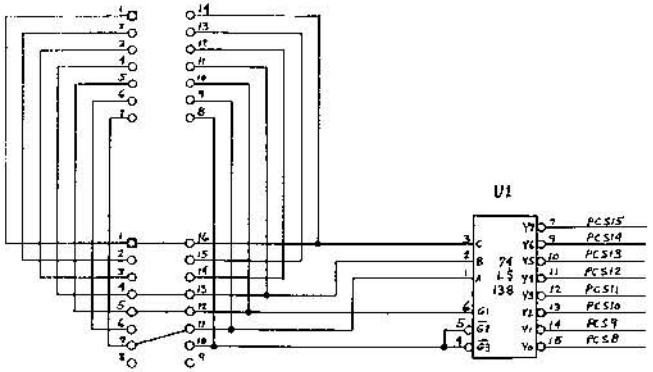


PROPRIETARY	DRAWN BY AKS	DATE 6-7-81	ENGINEER AKY	DATE 6-7-81	SHEET 5 OF 5	NEXT ASSEMBLY	USED ON	300 JAVA DR SUNNYVALE CA 94086 408-734-8400	SIZE D	TITLE AUDIO/COLOR PCB SCHEMATIC DIAGRAM	SHEET 5 OF 5	CODE	DRAWING NO 17-3387-11	REV B
	CHECKED AKS	DATE 6-22-81	PROJECT ENGR AKY	DATE 6-7-81										

NOTES: 1. For EPROMS +5V (VCC) = PIN 24
GND = PIN 12

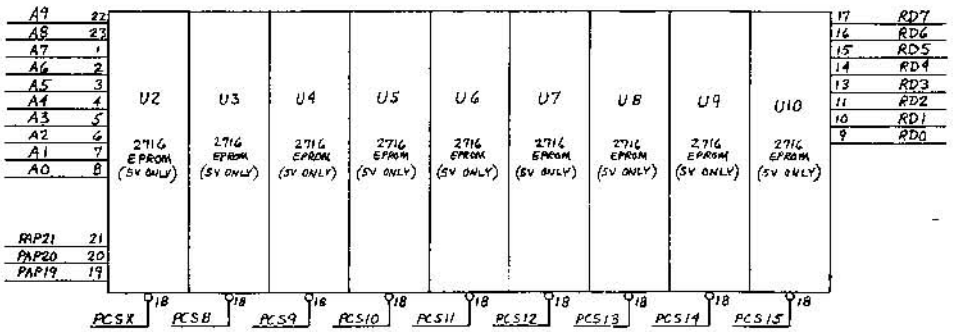
2. 10 ea. BYPASS CAPS NOT SHOWN,
Between +5VDC and GND. VALUE = .1μF 10V(min)
(Ceramic OK)

J1
14 PIN DIP SOCKET
(FROM LOGIC PCB POSITION 4B)

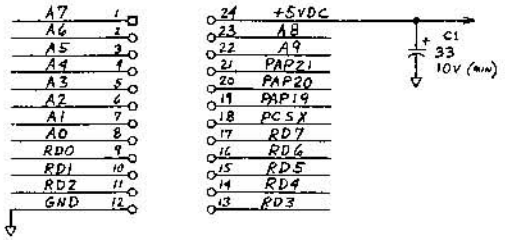


JPR1
16 PIN DIP PATTERN
w/JPRS included as shown
(may double as 16 PIN input socket)

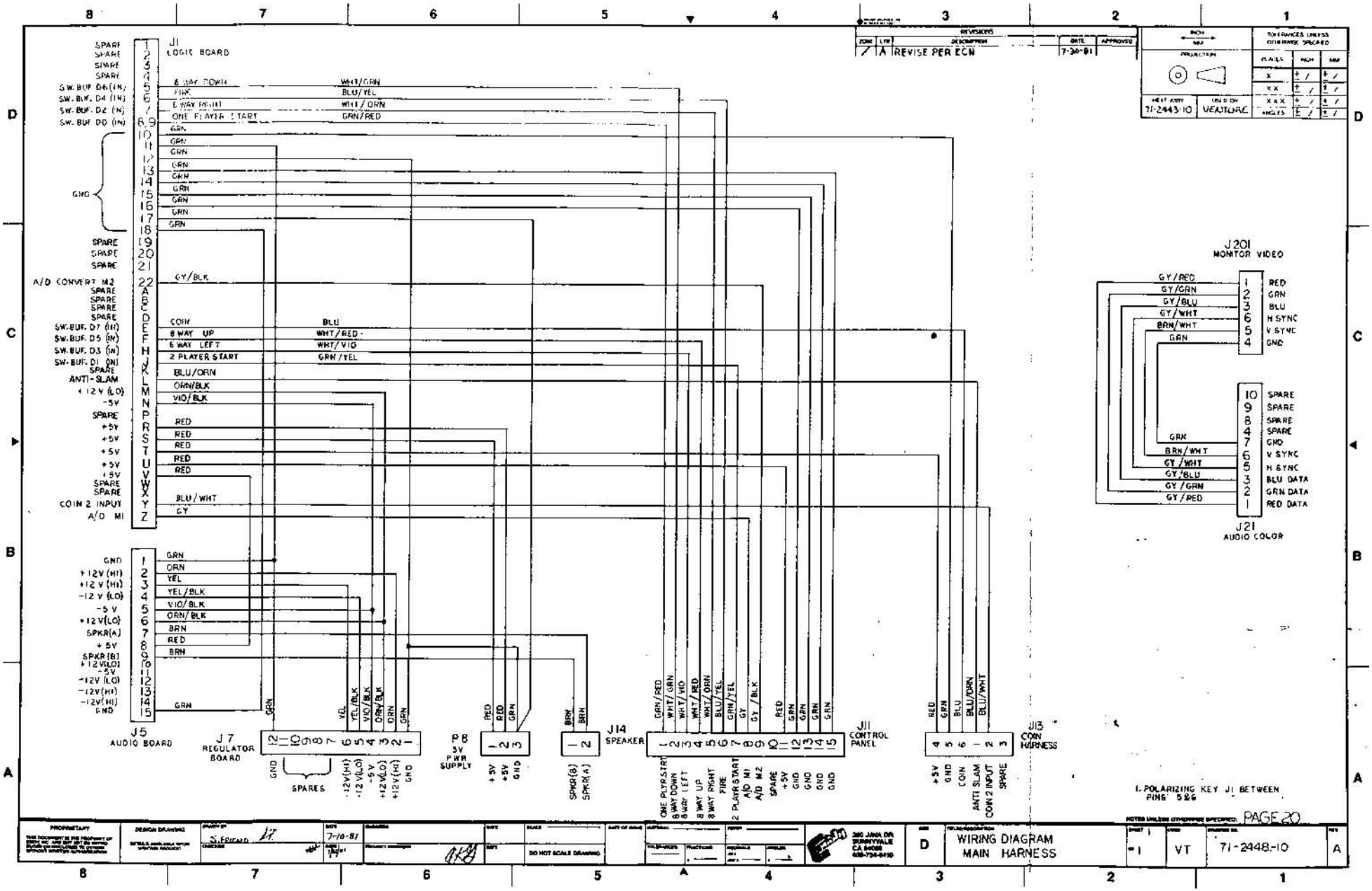
All lines BUSSED TOGETHER except CHIP SELECTS (PCSX, PCS8–PCS15)

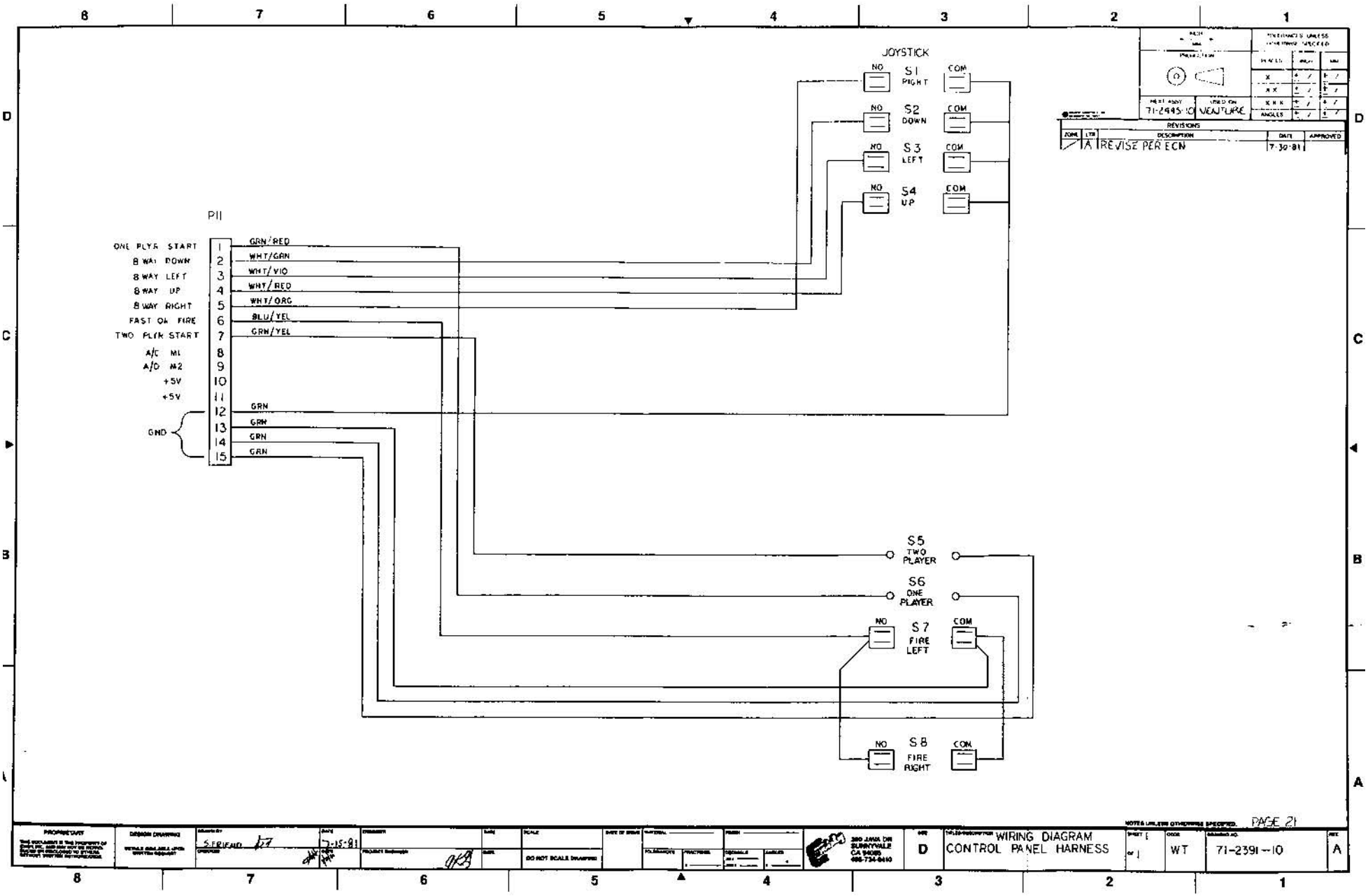


J2
24 PIN DIP SOCKET
(FROM LOGIC PCB POSITION 13A)



PROPRIETARY	DRAWN AKY 6-11-81	CHECKED AKY 6-11-81	SHEET 1 OF 1	NEXT ASSEMBLY 77-3374-11 REV E	USED ON 6502 LOGIC PCB FOR EXPANDED MEMORY	360 JAVA DR SUNNYVALE CA 94086 408-734-8410	SIZE D	MEMORY EXPANSION PCB (77-3389-11) SCHEMATIC	CODE	DRAWING NO. 77-3389-11	REV A
	APPROVED AKY 6-11-81	PROJECT ENGINEER AKY 6-11-81									


J1
LOGIC BOARD
SPARE
SPARE
SPARE
SPARE
SW. BUF. D6 (IN)
SW. BUF. D4 (IN)
SW. BUF. D2 (IN)
SW. BUF. D0 (IN)
GND
SPARE
SPARE
SPARE
A/D CONVERT M2
SPARE
SPARE
SPARE
SW. BUF. D7 (IN)
SW. BUF. D5 (IN)
SW. BUF. D3 (IN)
SW. BUF. D1 (IN)
SPARE
ANTI-SLAM
+12 V (LO)
-5V
SPARE
+5V
+5V
+5V
+5V
+5V
SPARE
SPARE
COIN 2 INPUT
A/D MI
8 WAY DOWN
FIRE
8 WAY RIGHT
ONE PLAYER START
GRN
GRN
GRN
GRN
GRN
GRN
GRN
GRN
GY/BLK
COIN
8 WAY UP
8 WAY LEFT
2 PLAYER START
BLU/ORN
ORN/BLK
VIO/BLK
RED
RED
RED
RED
RED
BLU/WHT
GY
BLU
WHT/RED
WHT/VIO
GRN/YEL
J5
AUDIO BOARD
GND
+12V (HI)
+12 V (HI)
-12 V (LO)
-5 V
+12V(LO)
SPKR(A)
+5V
SPKR(B)
+12V(LO)
-5V
-12V (LO)
-12V(HI)
-12V(HI)
GND
GRN
ORN
YEL
YEL/BLK
VIO/BLK
ORN/BLK
BRN
RED
BRN
GRN
J7
REGULATOR BOARD
GND
SPARES
-12V(HI)
-12 V(LO)
-5V
+12V(LO)
+12V(HI)
GND
P8
5V PWR SUPPLY
+5V
+5V
GND
SPKR(B)
SPKR(A)
J14
SPEAKER
J11
CONTROL PANEL
ONE PLYR START
8 WAY DOWN
8 WAY LEFT
8 WAY UP
8 WAY RIGHT
FIRE
2 PLAYR START
A/D MI
A/D M2
SPARE
+5V
GND
GND
GND
GND
J13
COIN HARNESS
+5V
GND
COIN
ANTI SLAM
COIN 2 INPUT
SPARE
J201
MONITOR VIDEO
RED
GRN
BLU
H SYNC
V SYNC
GND
SPARE
SPARE
SPARE
SPARE
GND
V SYNC
H SYNC
BLU DATA
GRN DATA
RED DATA
J21
AUDIO COLOR
1. POLARIZING KEY J1 BETWEEN PINS 5&6
REVISIONS
REVISE PER ECN
7-30-81
WIRING DIAGRAM
MAIN HARNESS
71-2448-10
PAGE 20



REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REVISE PER ECN	7-30-81	

NEXT ASSY 71-2495-10 USED ON VECTOR

PROPRIETARY

DESIGN DRAWING

S. FRIEND 7-15-81

DO NOT SCALE DRAWING

SIZE D

TITLE/DESCRIPTION WIRING DIAGRAM CONTROL PANEL HARNESS

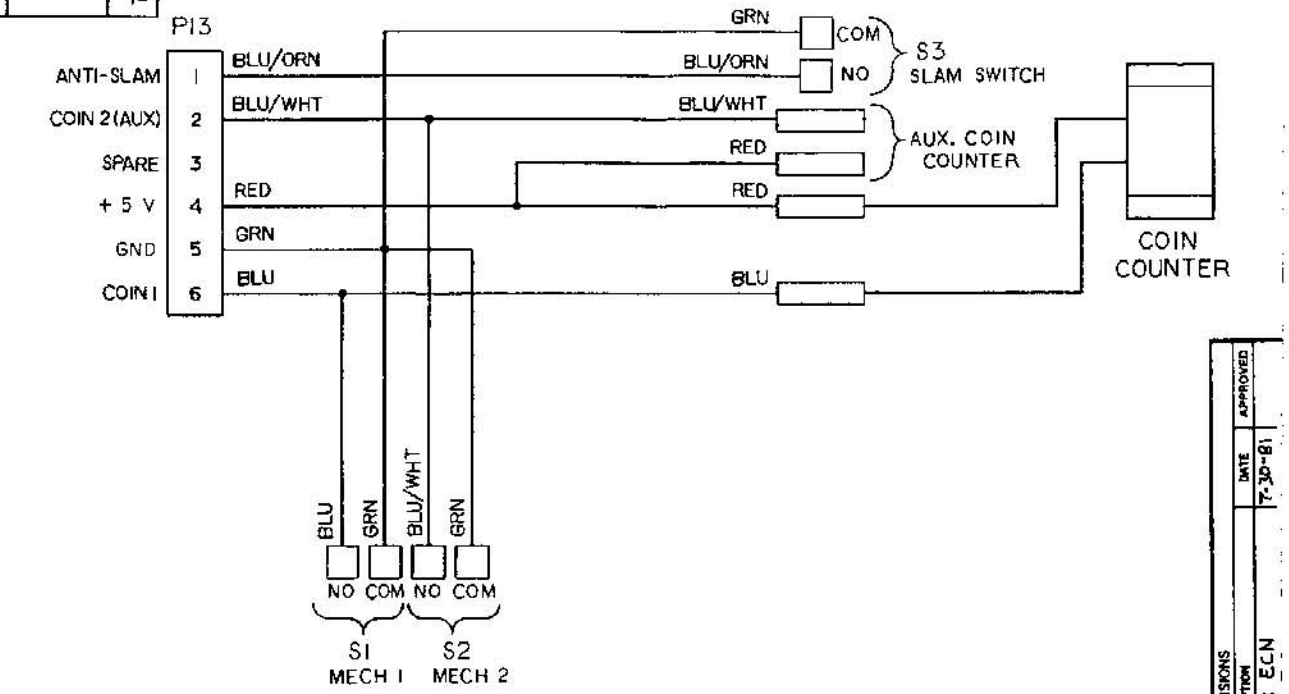
SHEET 1 OF 1

CODE WT

DRAWING NO. 71-2391-10

REV A

NOTES UNLESS OTHERWISE SPECIFIED.



ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED
	A	REVISED AS PER ECN	7-30-81	

PAGE 22

NOTES UNLESS OTHERWISE SPECIFIED:

SIZE C	TITLE/DESCRIPTION: WIRING DIAGRAM-UNIV. COIN DOOR HARNESS	SHEET 1 OF 1	
CODE VT	DRAWING NO. 71-2449-10	REV A	
SCALE —	DO NOT SCALE DRAWING		

DRAWN BY
CHECKED
ENGINEER
PROJECT ENGINEER
MFG

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DESIGN DRAWING
DETAILS AVAILABLE UPON WRITTEN REQUEST

MATERIAL

TOLERANCES
FRACTIONS ± —
ANGLES ± —
DECIMALS .XX ± — .XXX ± —

TOLERANCES UNLESS OTHERWISE SPECIFIED

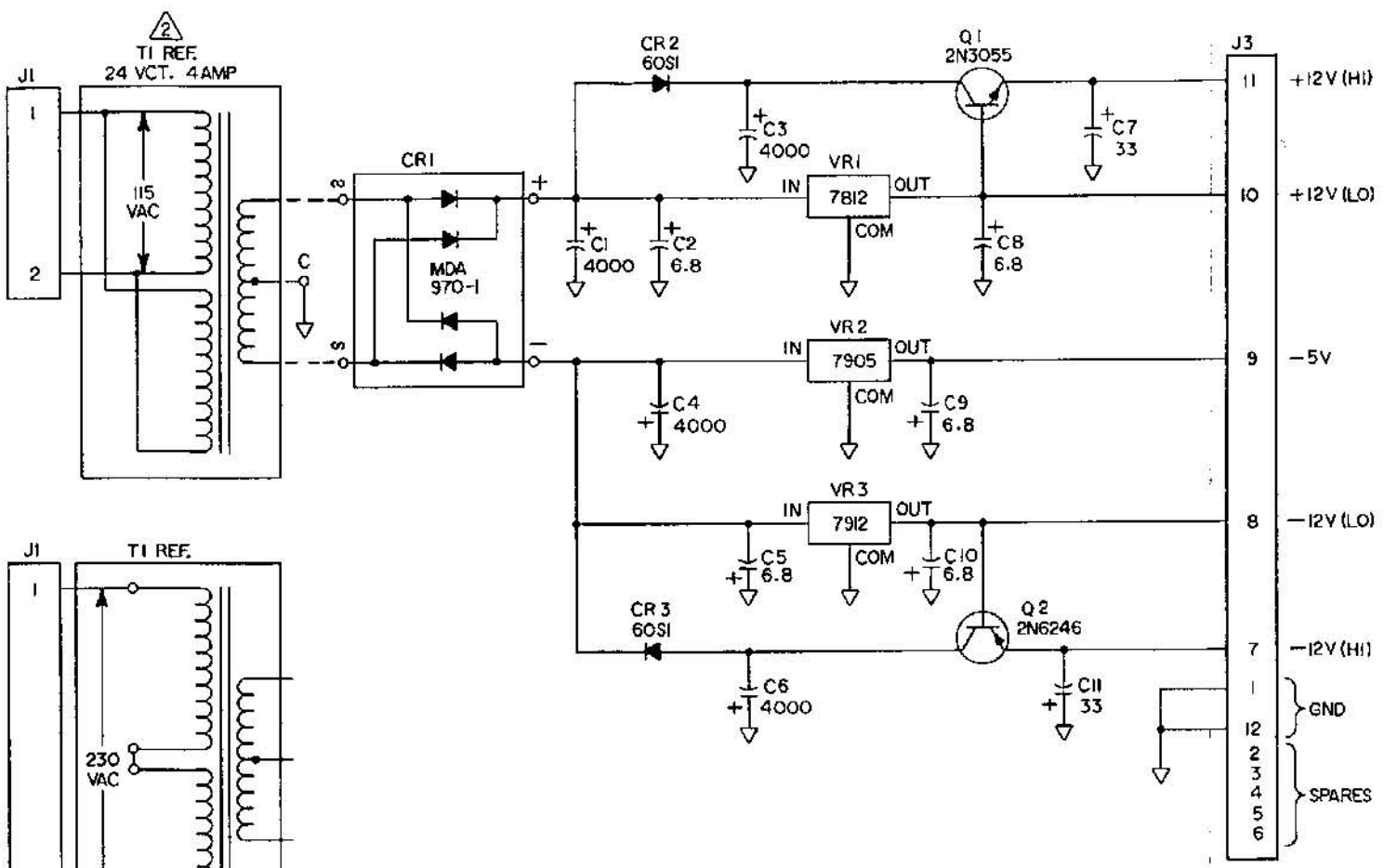
PLACES	INCH	MM
X	± /	± /
XX	± /	± /
XXX	± /	± /
ANGLES	± /	± /

INCH ↔ MM
PROJECTION

USED ON VEGTURE
NEXT ASSY 71-2444-10

ATARI
380 JAVA DR
SUNNYVALE
CA 94086
408-734-9410

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
/	H	REVISED PER ECN	7-30-81	



2 SHOWN FOR REFERENCE ONLY
1. ALL CAPACITOR VALUES ARE IN MICROFARADS

NOTES UNLESS OTHERWISE SPECIFIED:

TITLE/DESCRIPTION: ELECTRICAL SCHEMATIC, UNIVERSAL POWER SUPPLY
DRAWING NO. 77-3365-11
REV H
SIZE C
CODE VT
SHEET 1 OF 1
SCALE —
DATES 7-10-81 7/16/81 9/15/81
DRAWN BY
CHECKED
ENGINEER
MFG/QUALITY ENGINEER
PROJECT ENGINEER
MATERIAL
FINISH
TOLERANCES
FRACTIONAL ±
ANGLES ±
.XX ±
.XXX ±

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DESIGN DRAWING DETAILS AVAILABLE UPON WRITTEN REQUEST

DO NOT SCALE DRAWING

PAGE 23

INCH / MM
PROJECTION
TOLERANCES UNLESS OTHERWISE SPECIFIED

PLACES	INCH	MM
.X	± /	± /
.XX	± /	± /
.XXX	± /	± /
ANGLES	± /	± /

NEXT ASSY 77-3365-15
USED ON VENTURE

EXOTIC
390 JAVA DR
SUNNYVALE
CA 94086
408-734-9410